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MS-7358 uATX Version: 1.0

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q35/G33 North Bridge
Intel ICH9 (DO/DH South Bridge)

On Board Device:

CLOCK Gen ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LPC TPM -- SLB9635
LAN -- INTEL NINEVEH/EKRON
HD Audio Codec -- ALC888
1394 Controller -- VT6308 (2-port)
PCIE to PATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

PWM: Intersil ISL6322 (4 Phases) w/ ISL6612 driver

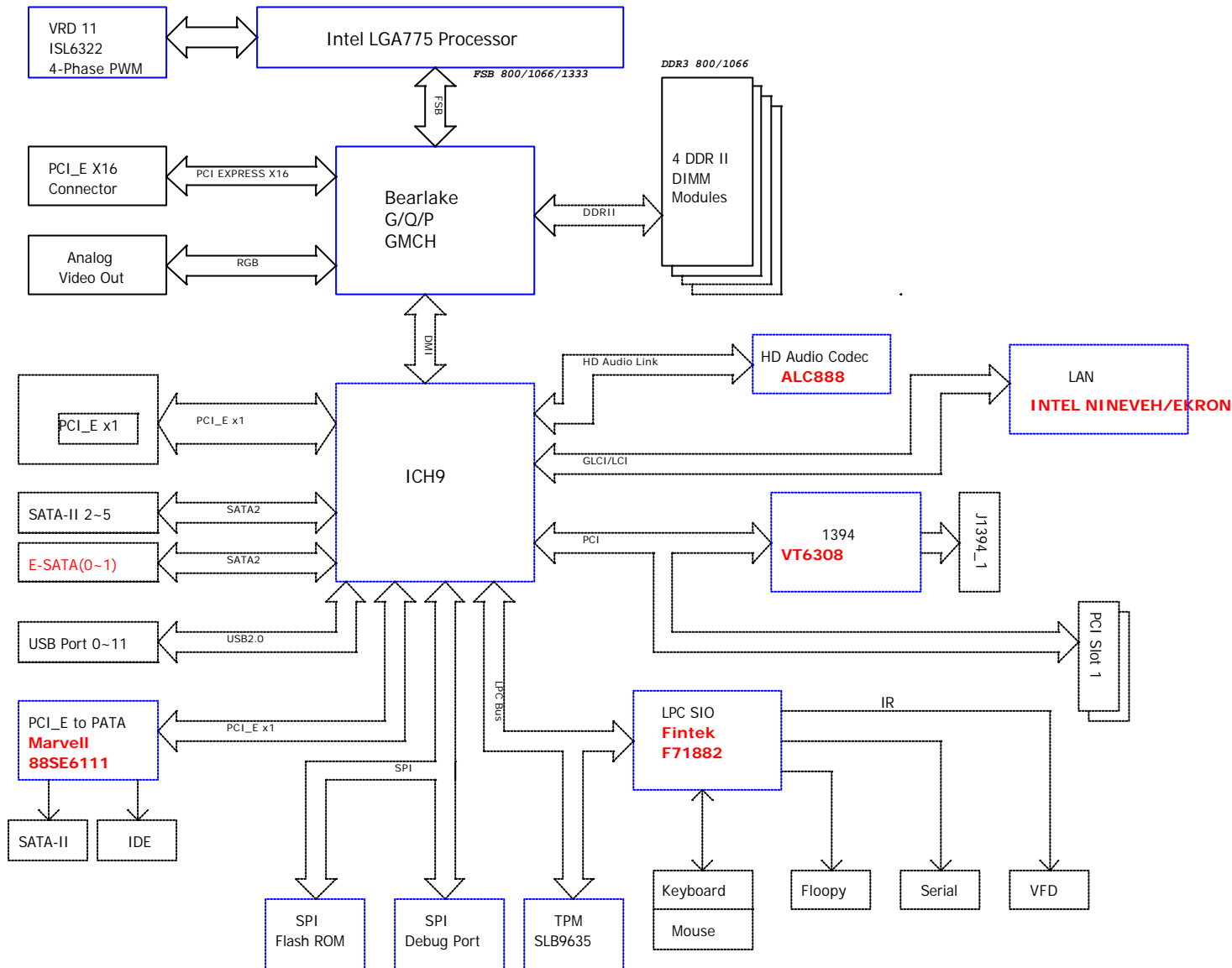
Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-Q33/ICH9DO	cfg-7358-STD	
VIIV	Bearlake-G33/ICH9DH	2007/08/29 cfg-7358-Viiv	601-7358-10S



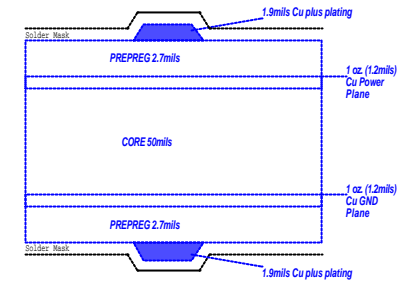
MICRO-STAR INT'L CO.,LTD			
MS-7358			
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Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



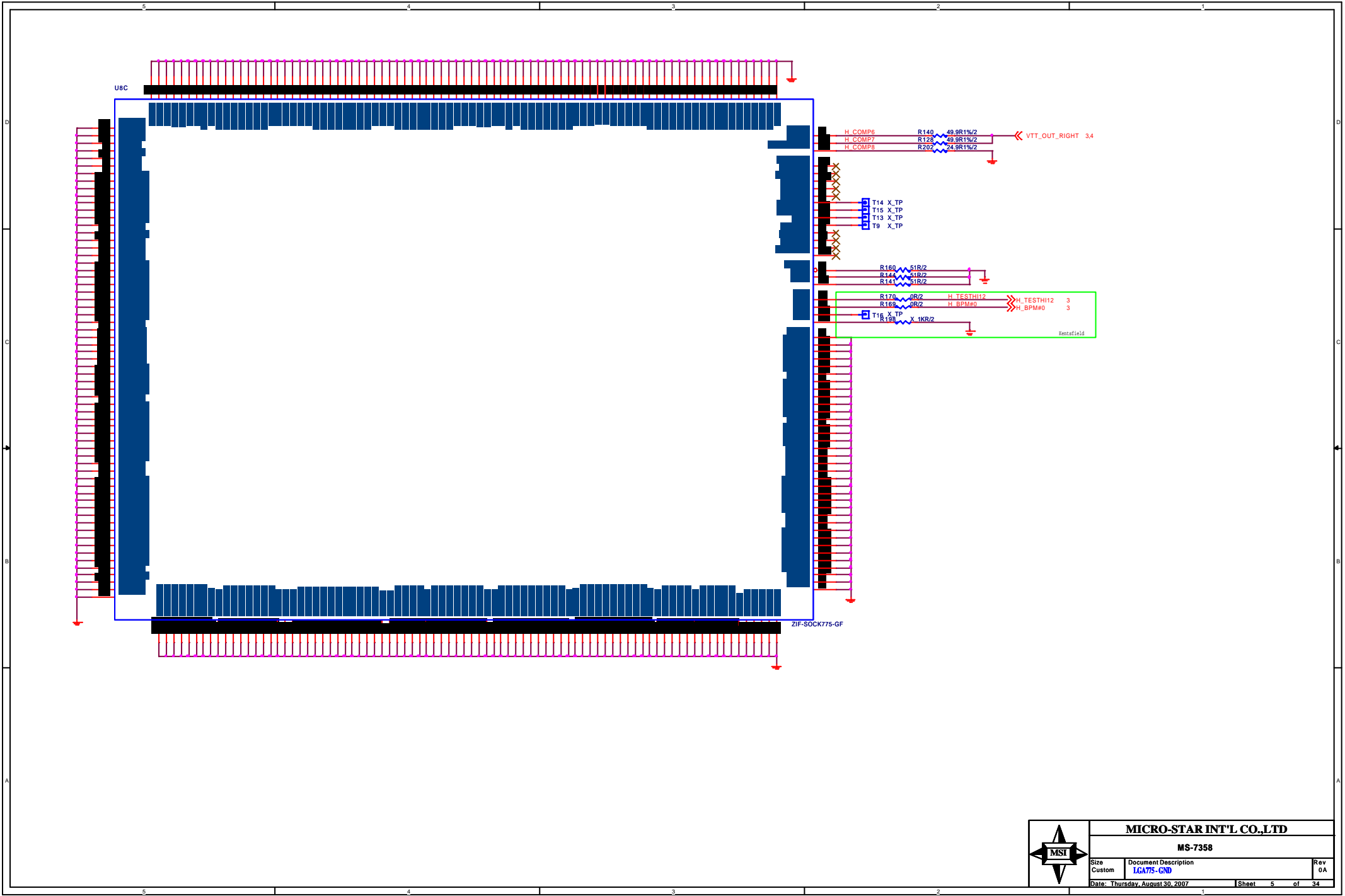
Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15



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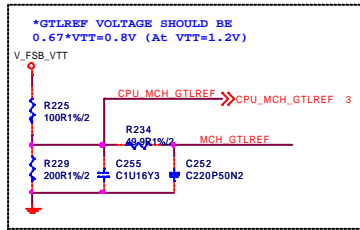
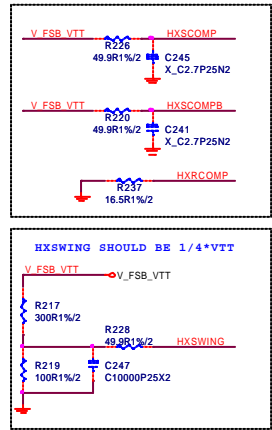
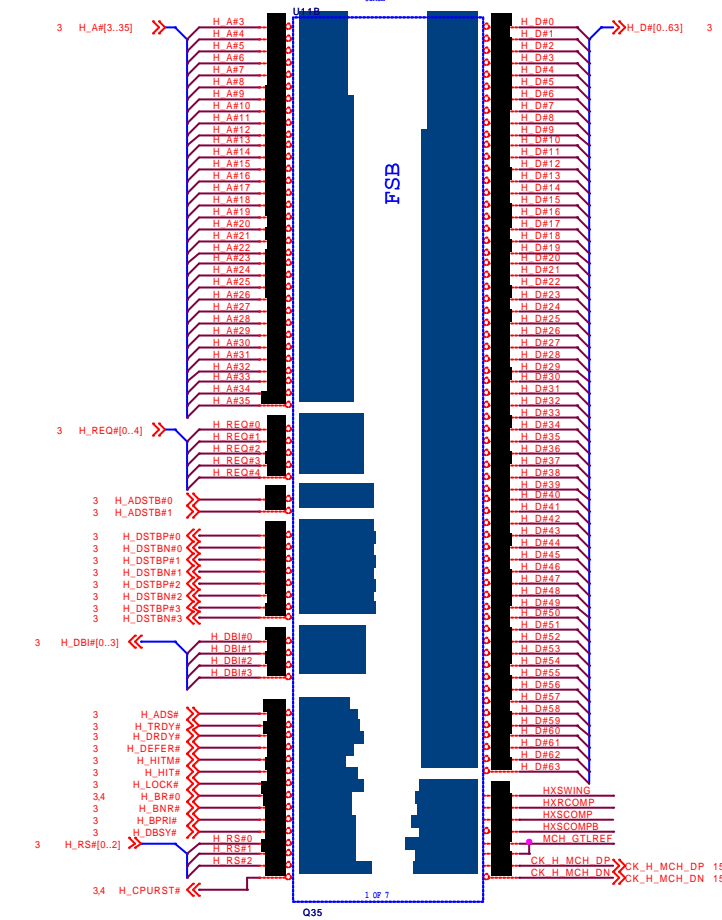
Size	Document Description	Rev
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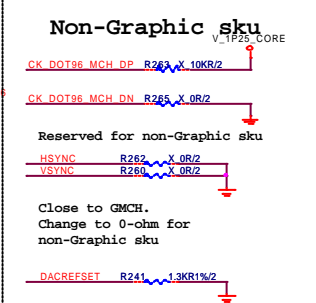
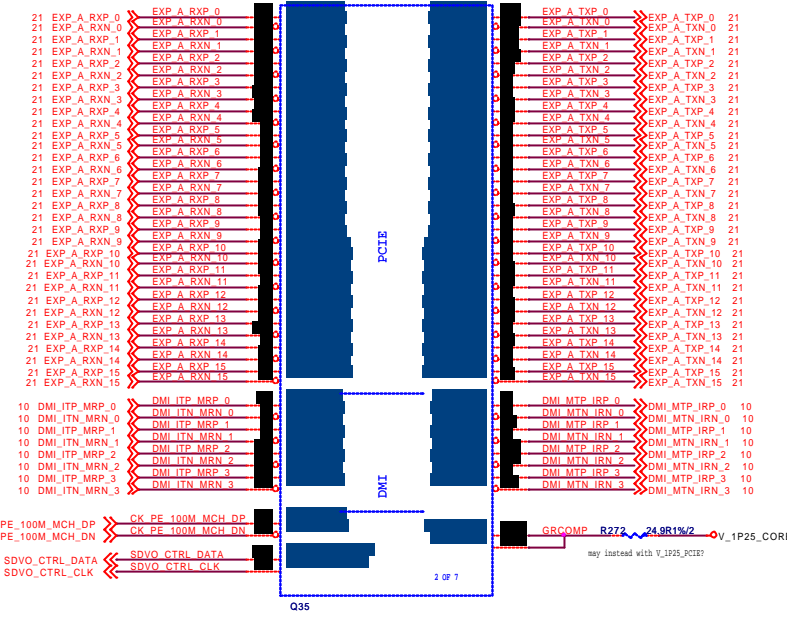
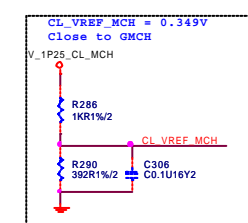
MS-7358

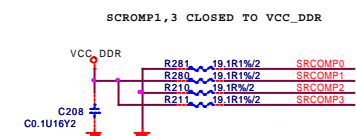
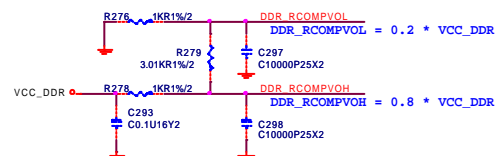
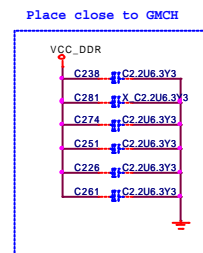
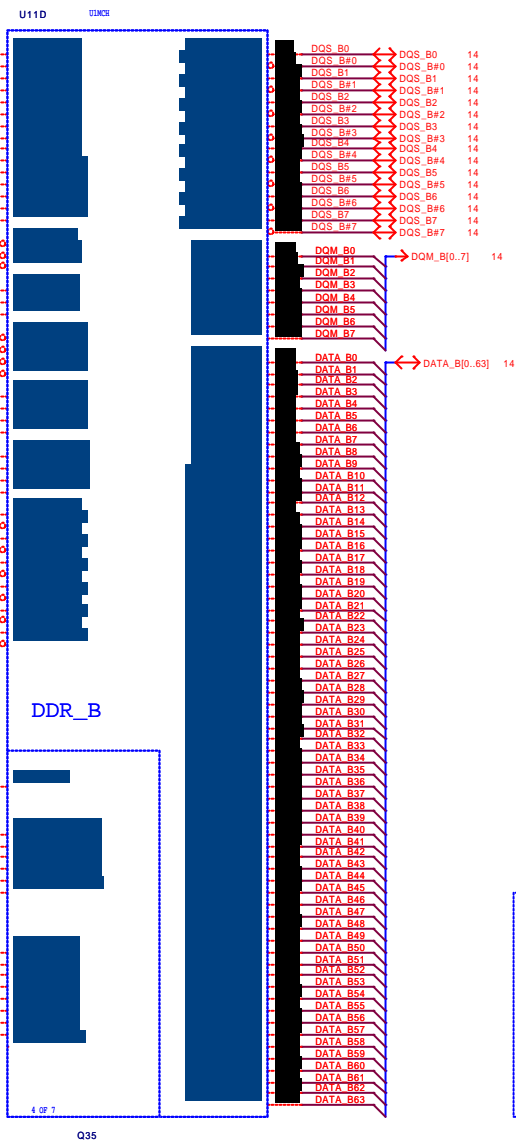
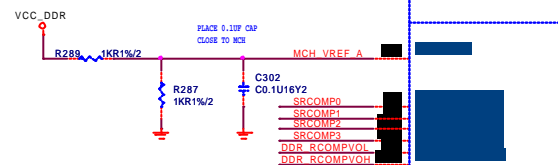
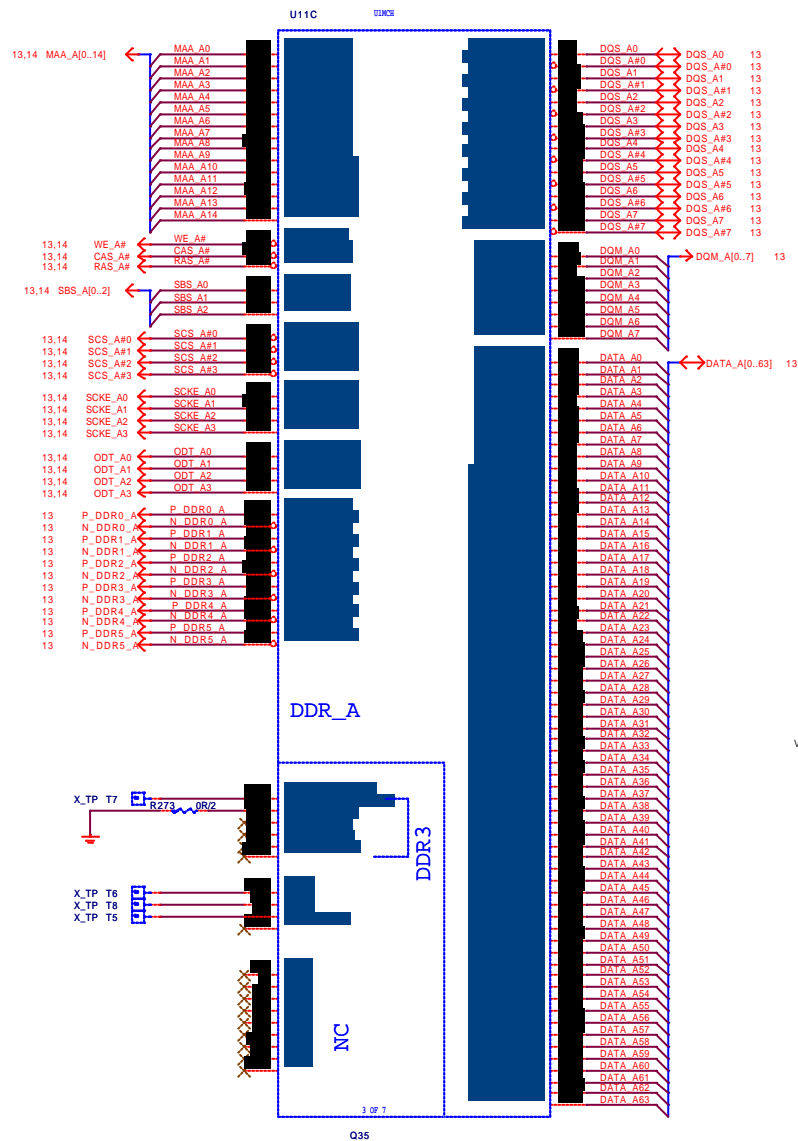
Size	Document Description	Rev
Custom	LGA775-GND	0A
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Really need or just reserve the invert?

Pin	W	E	Description
MTTPE	DDR2	DDR3	MEMORY TYPE
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SDVO co-existence
MCH_TGREN	Enable	Disable	TLS confidentiality



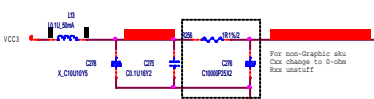
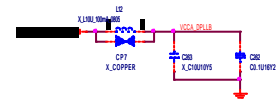
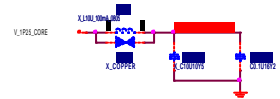
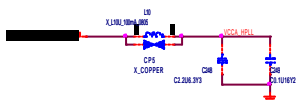
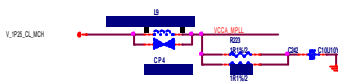
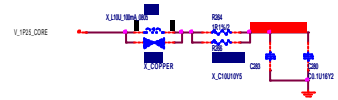


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NB POWER

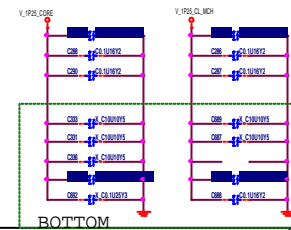
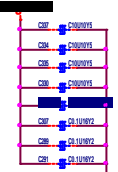
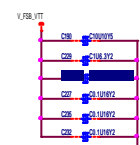
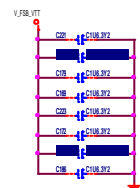
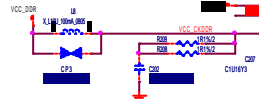
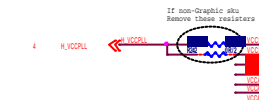
VCCO_CRT
For non-graphics sku
change to 0-ohm (1402)

VCCO_CRT
For non-graphics sku
change to 0-ohm (1403)



For non-graphics sku
change to 0-ohm
for start-up

POWER

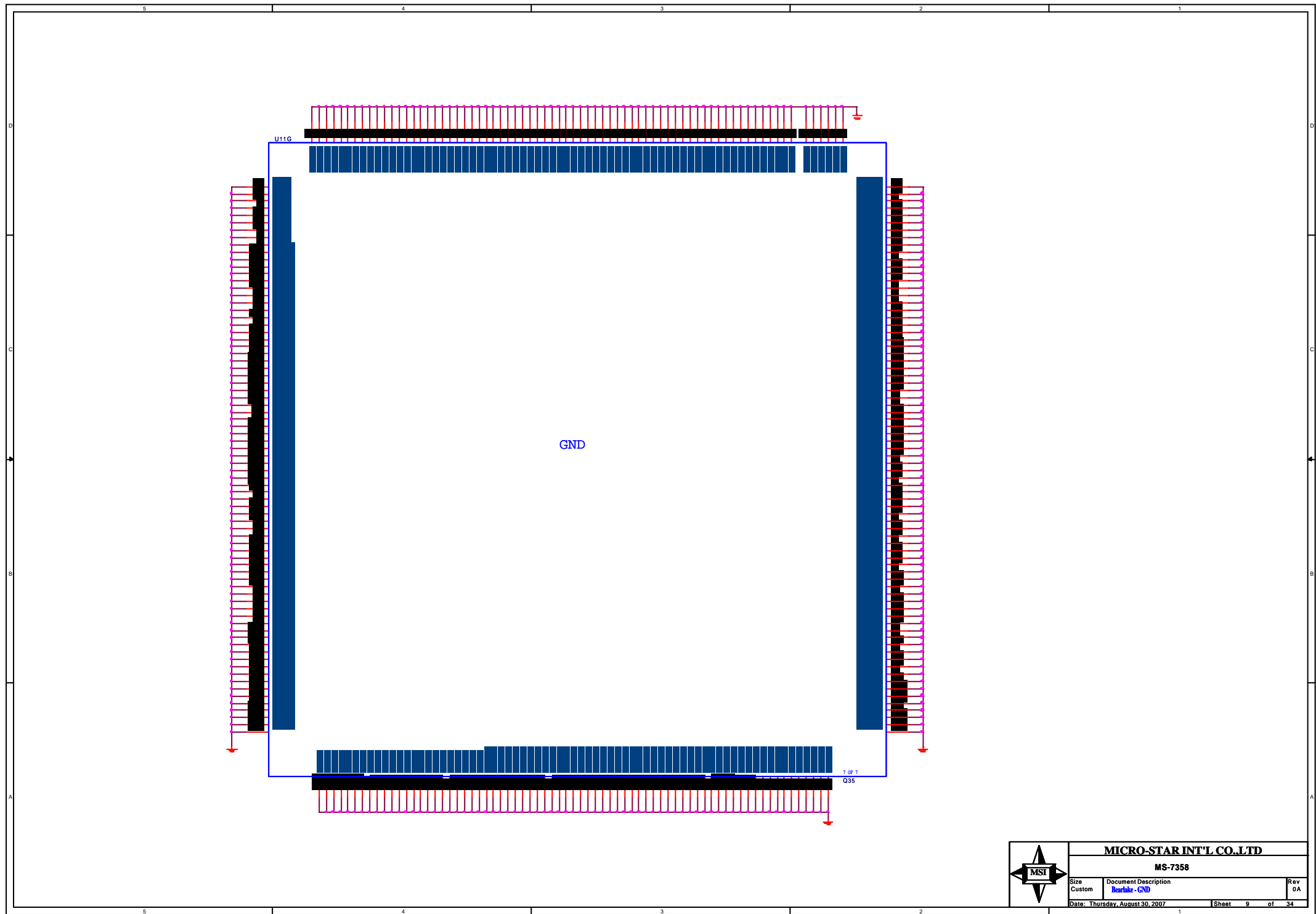


Separate when AMT is supported

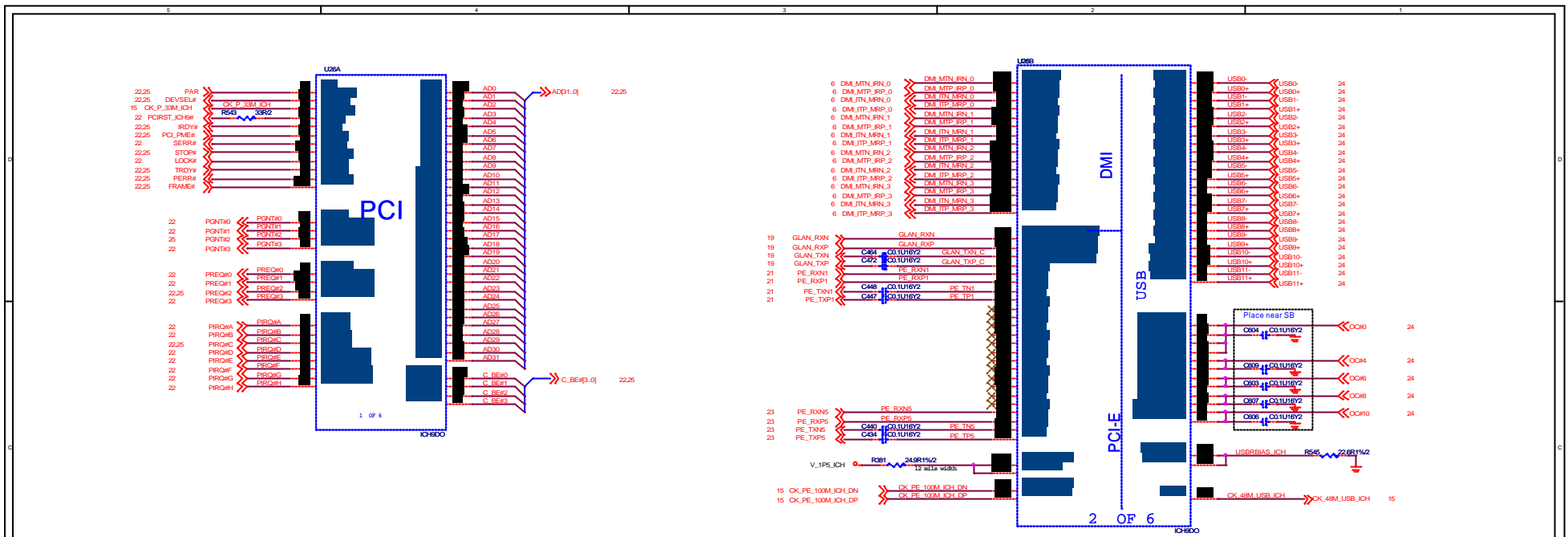
MICRO-STAR INT'L CO.,LTD

MS-735

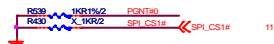
Beastlake - Power



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MS-7358			
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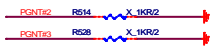


SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

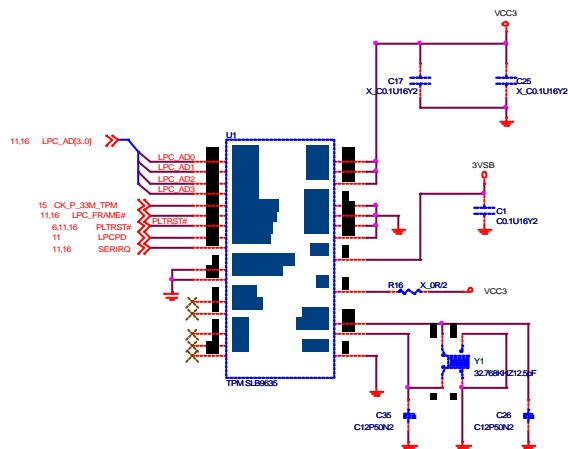
PQNT#(3:0) Internal Pull-up

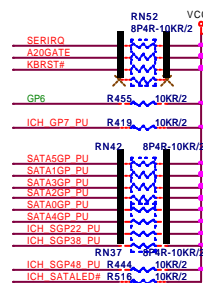
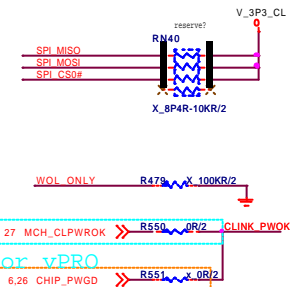
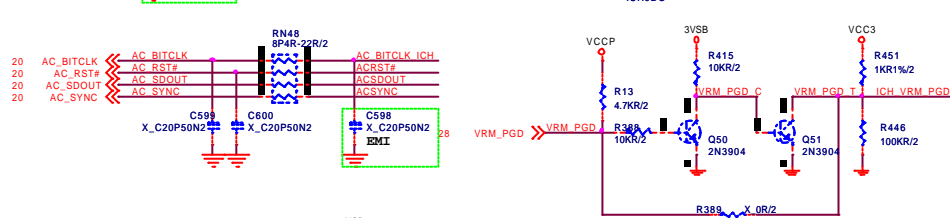
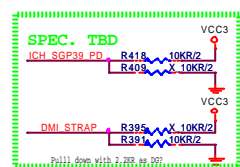
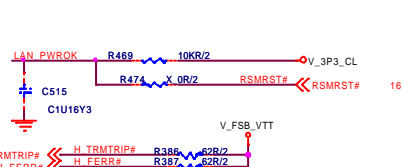
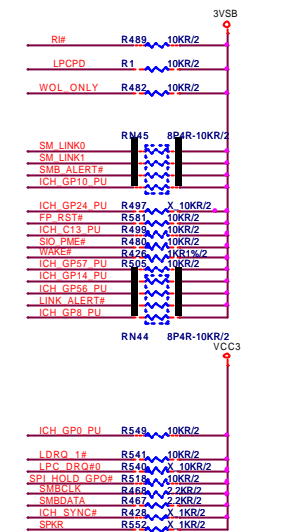


SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIe PORT CONFIG 2 BIT 0 (5-6)

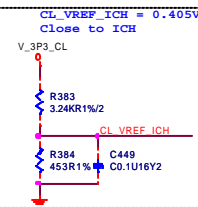
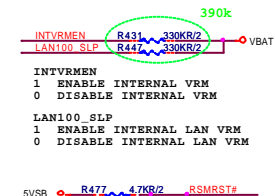
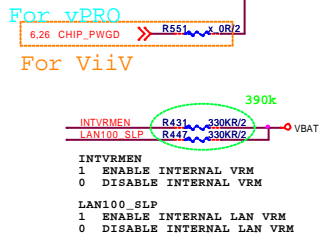
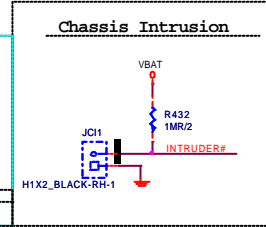
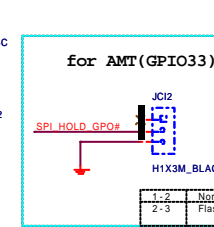
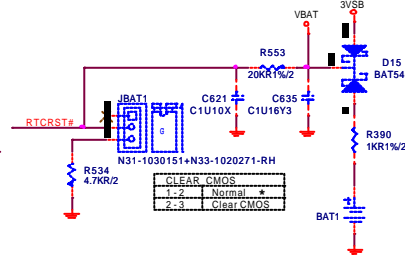
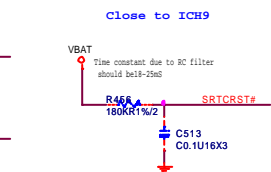
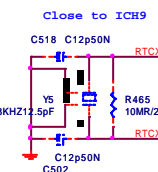
MSI BIOS/BIOS_Flash strap PCI_E port configuration bit[1:0]. Internal weak pull down.
00:10:10:10:10:10 11:00:00:00:00:00

TPM - Security Controller

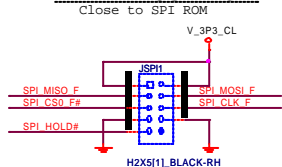




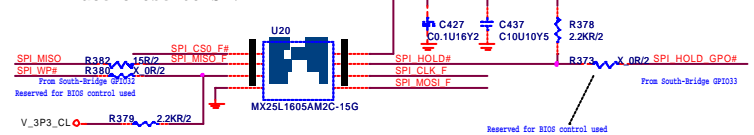
RTC Block



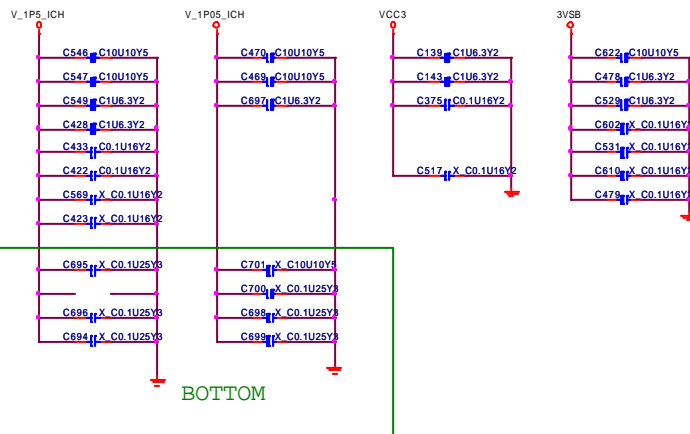
SPI DEBUG PROT



SPI FLASH ROM
Place close to SB.



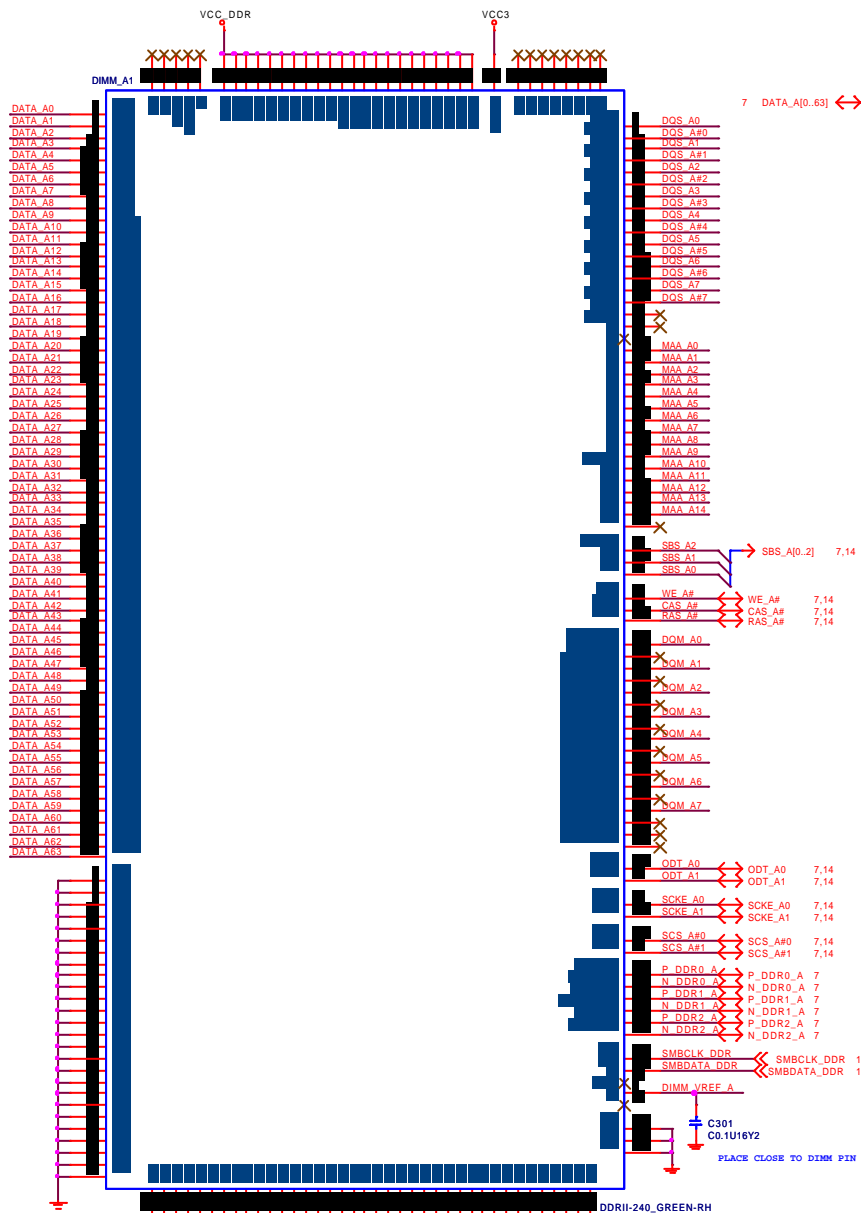
V5REF must be powered up before VCC3 or after VCC3 within 0.7V.
Also, V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and JVS8.
However, the JVS8 is derived from the SVS8 on the power supply
thru a voltage regulator and therefore, they can satisfy the requirement.



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0A

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DDRII DIMM_A1



SMBCLK_DDR R76 33R/2

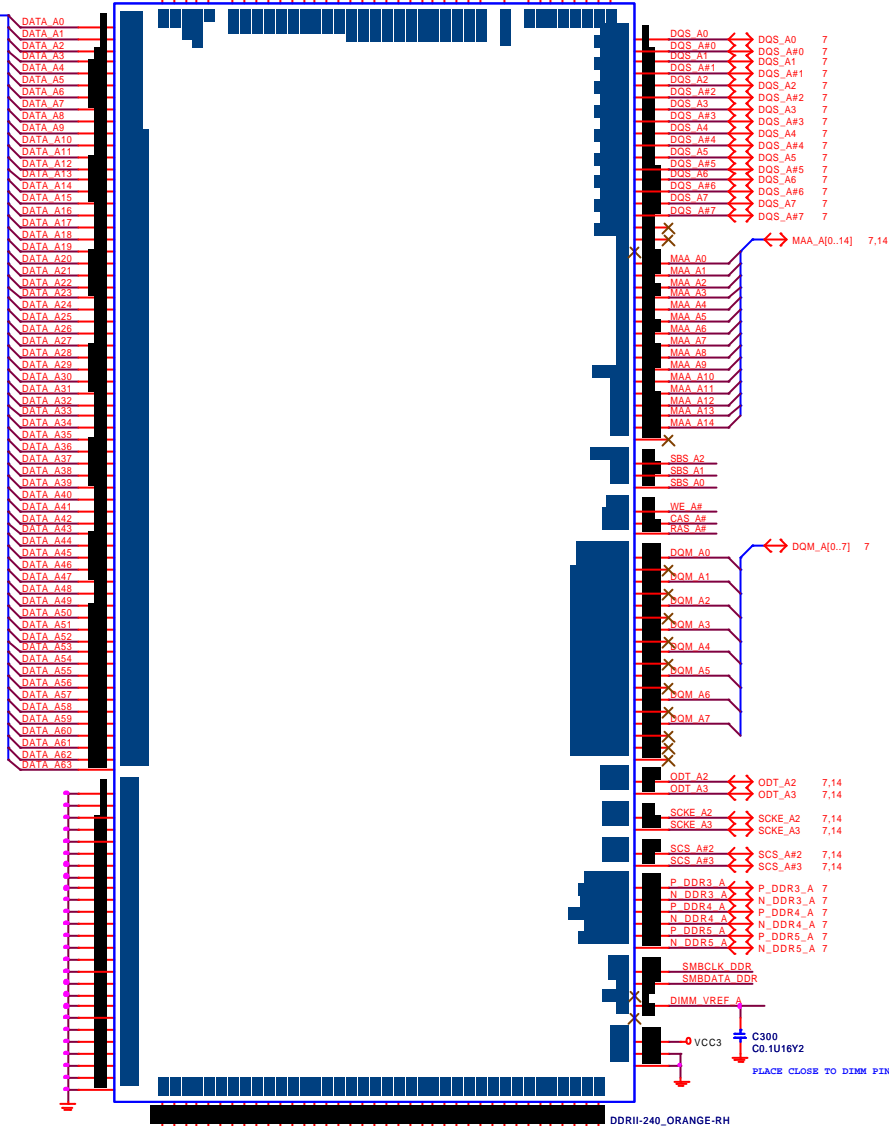
SMBDATA_DDR R80 33R/2

SMBCLK

SMBDATA

11,15,21,26,28

11,15,21,26,28



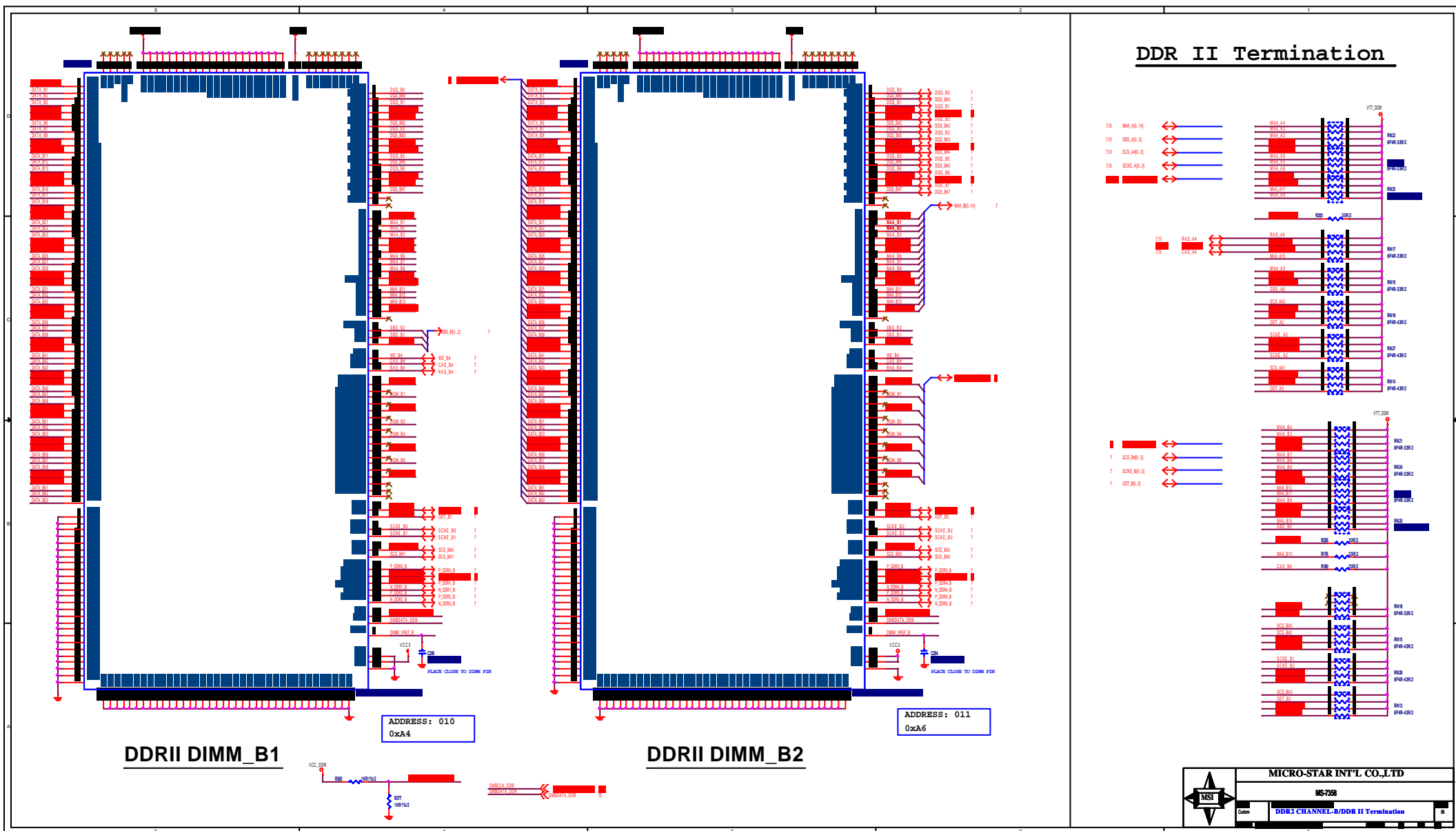
DDRII DIMM_A2

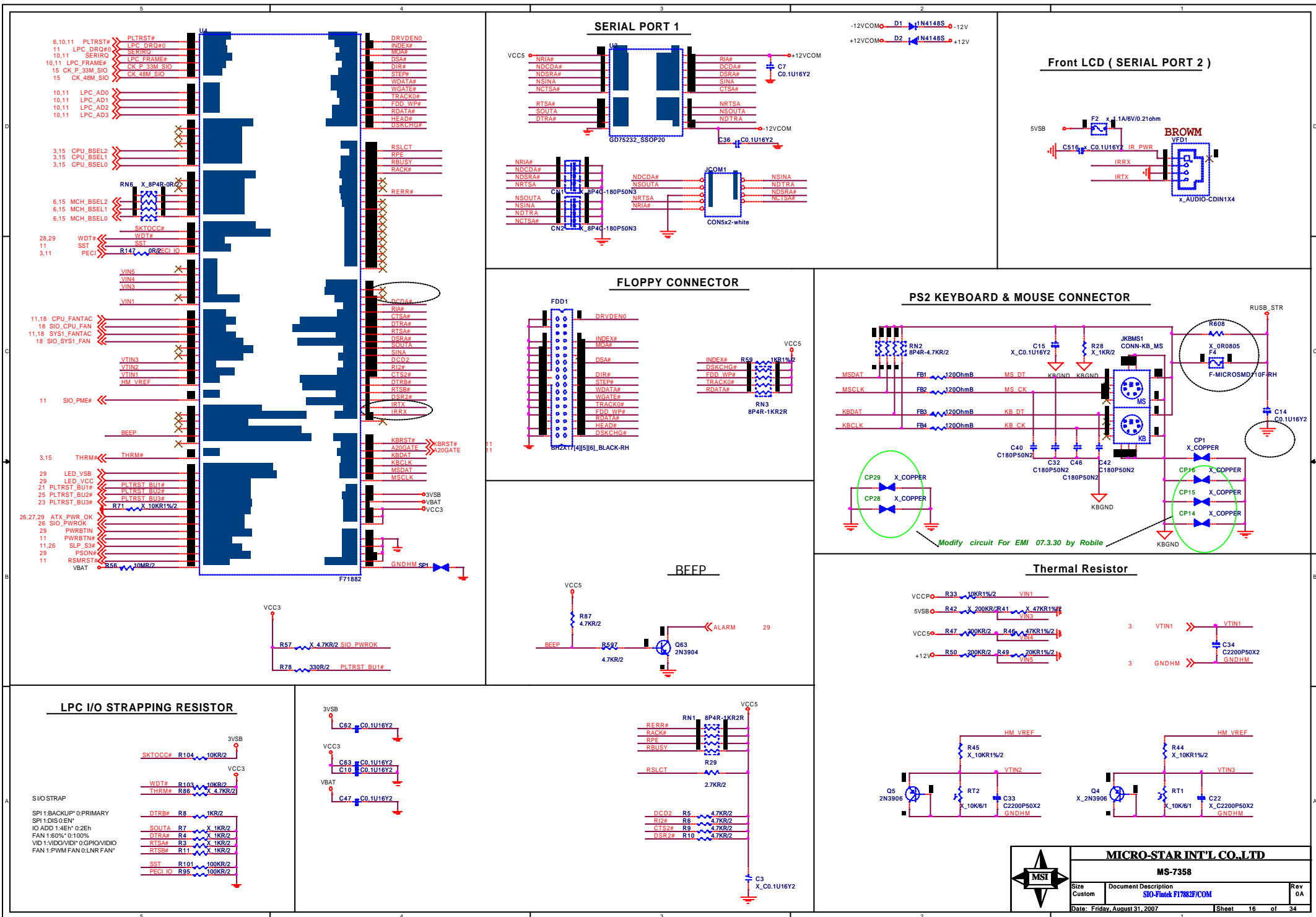


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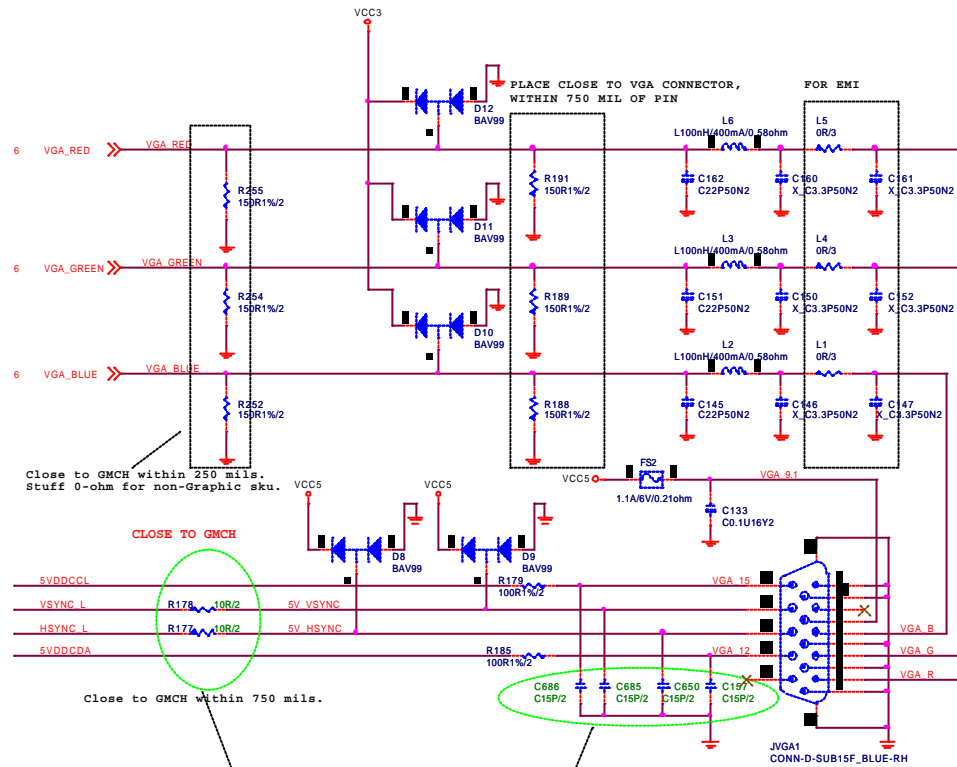
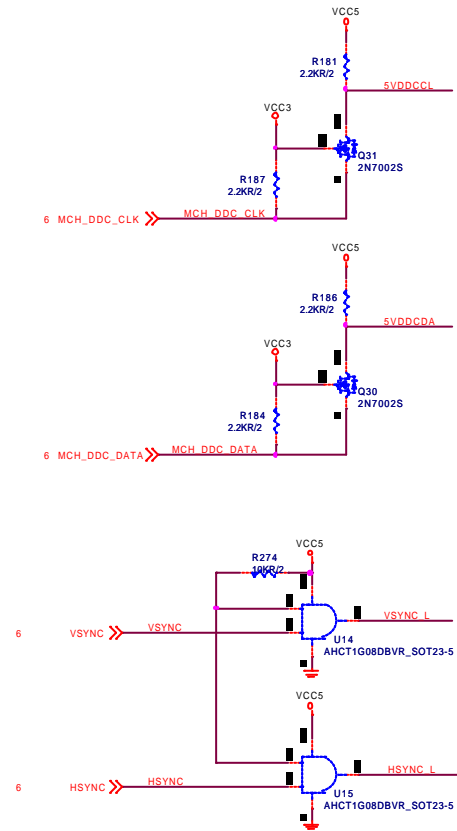
MS-7358

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Custom	DDR2 CHANNEL-A	0A
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Video Connector



Close to GMCH within 250 mils.
Stuff 0-ohm for non-Graphic sku.

CLOSE TO GMCH

Close to GMCH within 750 mils.

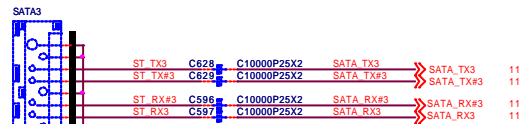
Modify HSYNC/VSYNC Circuit
1. R178, R177 from 30R to 10R
2. CN3 from 33p to 15p
For Rise time edge not clean 07.3.30 by Robile



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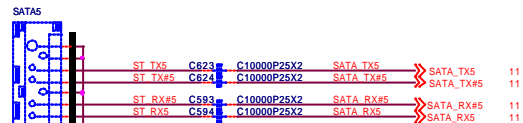
Size	Document Description	Rev
Custom	VGA	0A
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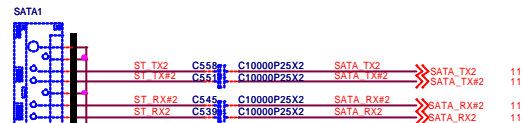
CONN-SATA10P_PURPLE



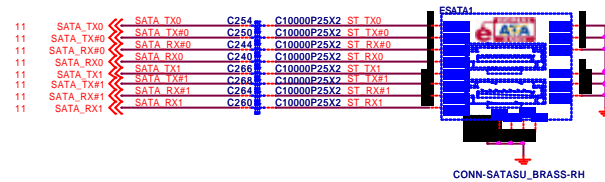
CONN-SATA10P_PURPLE



CONN-SATA10P_PURPLE



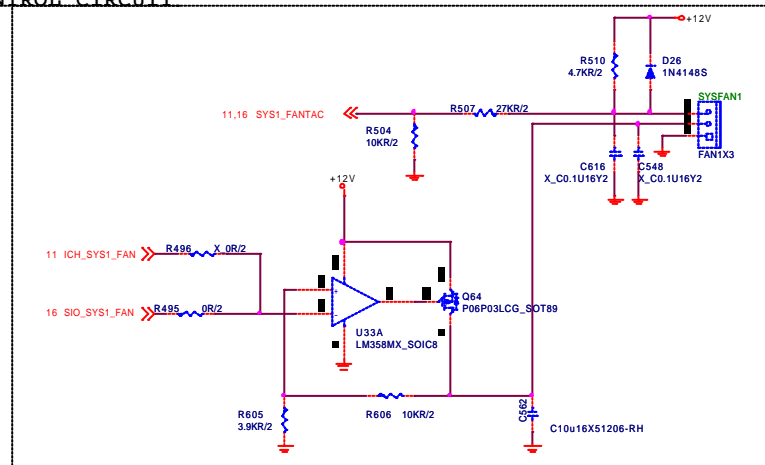
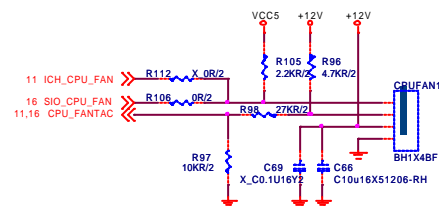
CONN-SATA10P_PURPLE



CONN-SATASU_BRASS-RH

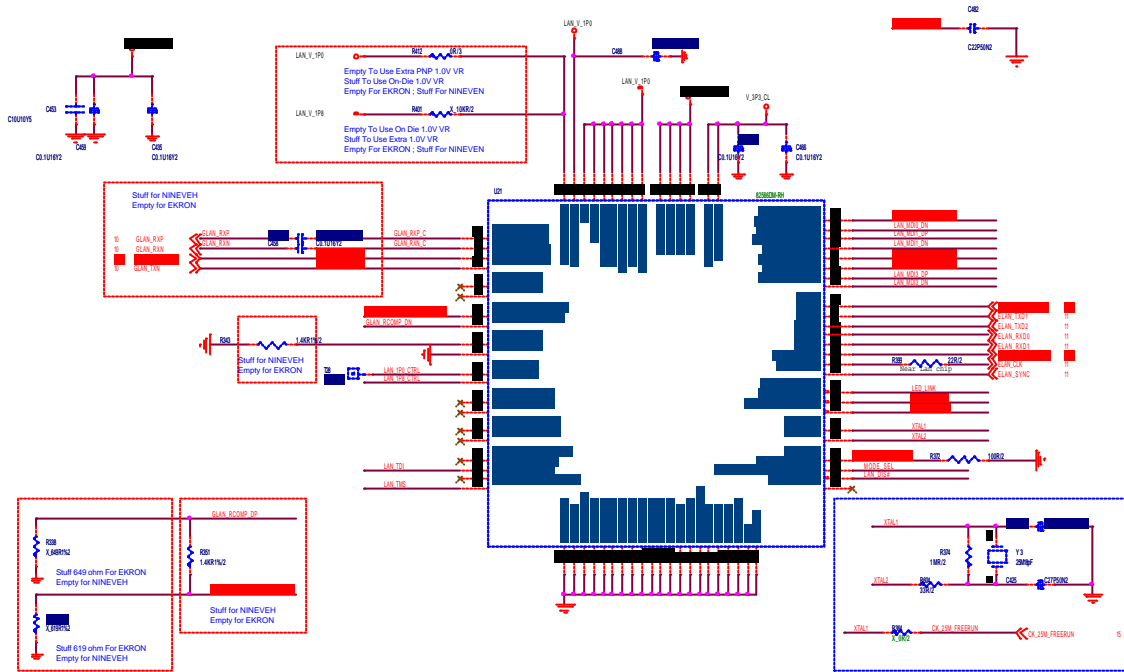
e-SATA trace length should be less than 10 inch.(Connector to Chip)

FAN-COUNTROL CIRCUIT



Modify System FAN circuit & Remove PWR FAN for spec need 3pin DC Smart FAN 07.3.30 by Robile

LAN - NINEVEH/EKRON



Intel i2256DM
For business desktop PCs.Support Intel AMT2 or ASF 2.0 alerting,Circuit Breaker,WoL_PXE,Multipoint teaming,RSS,Intel Stable Image Platform Program drivers.
Intel i2256DC
For consumer desktop PC.Support Digital Home capabilities,WoL_PXE.
Intel i225G2V
Basic 10/100 Ethernet connection.
B06-425605-116
FOR MECP CONSIGN,CHIP LAN,INTEL82566DM_BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE
B06-425605-15-00
_CHIP LAN,INTEL82566DC_BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE
B06-425605-00-00
_CHIP LAN,INTEL82562V_BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

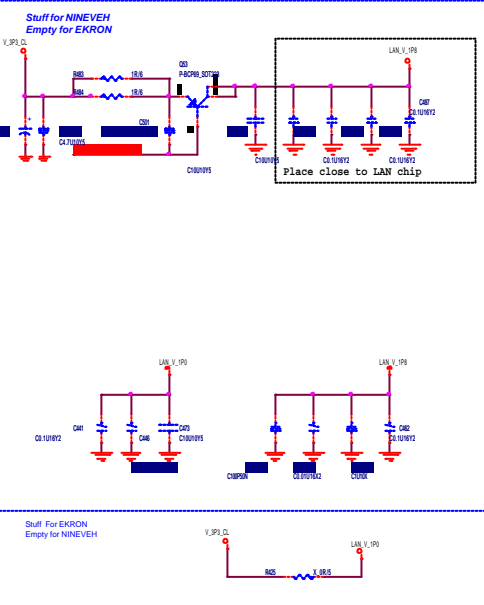
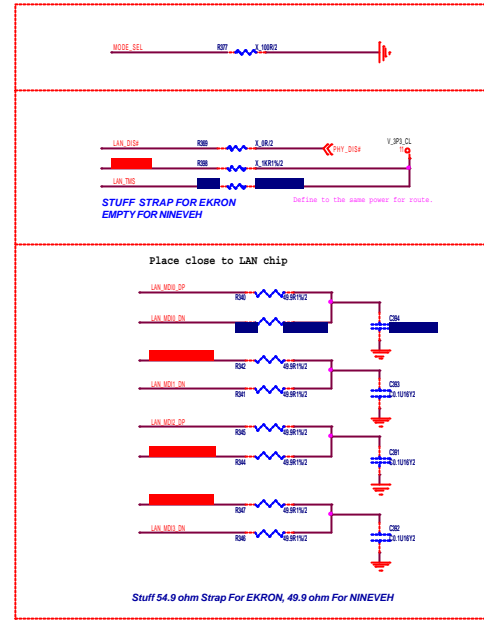
Modify Lan CLK circuit only BOM changes 07.3.30 by Robile

Speed LED Type
100Mbps : Orange
100Mbps : Green
10Mbps : LED off

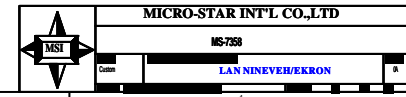
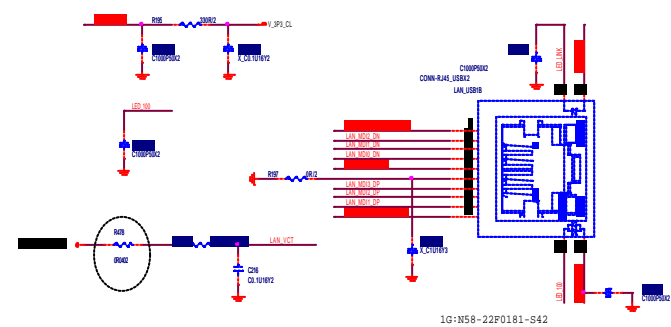
YELLOW : For Active/Link

ACT_LED	Link_LED
S1/S3/S4/S5: HIGH	S6: HIGH
	S1/S3/S4: WOL EN→LOW WOL DIS→HIGH

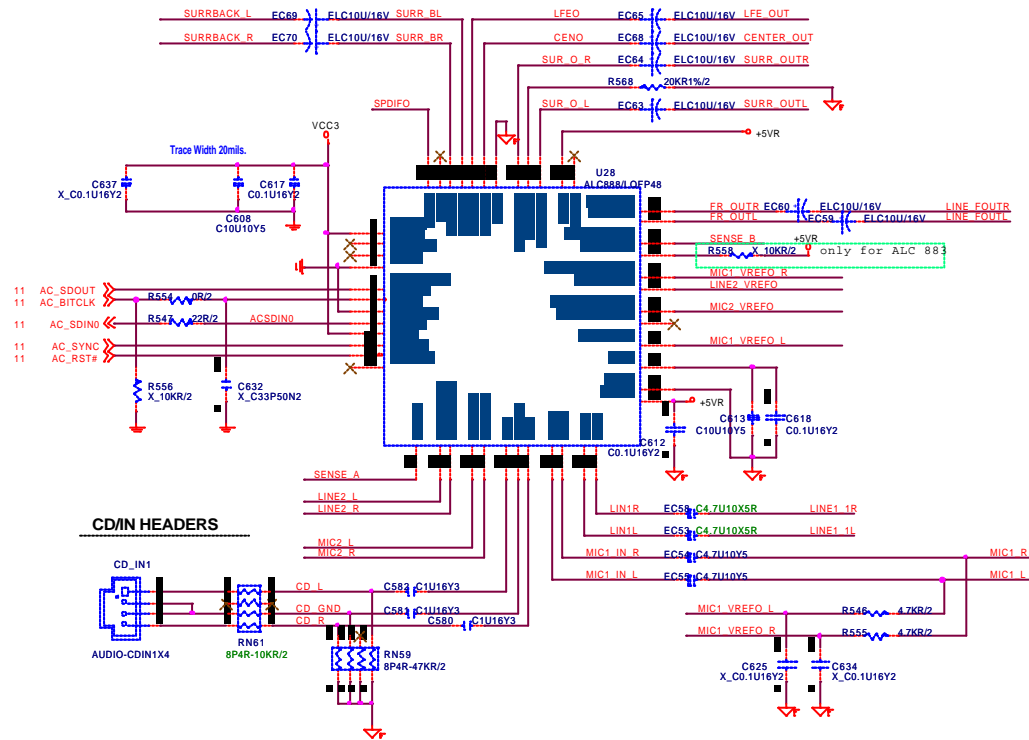
Giga-Lan	10/100-Lan
N58-22F0181-842	N58-22F0061-842
N58-22F0061-P02	N58-22F0061-P02
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	10 None
19 Yellow	19 Yellow
20 Yellow	20 Yellow
21 Orange	21 Orange
22 Green	22 Green



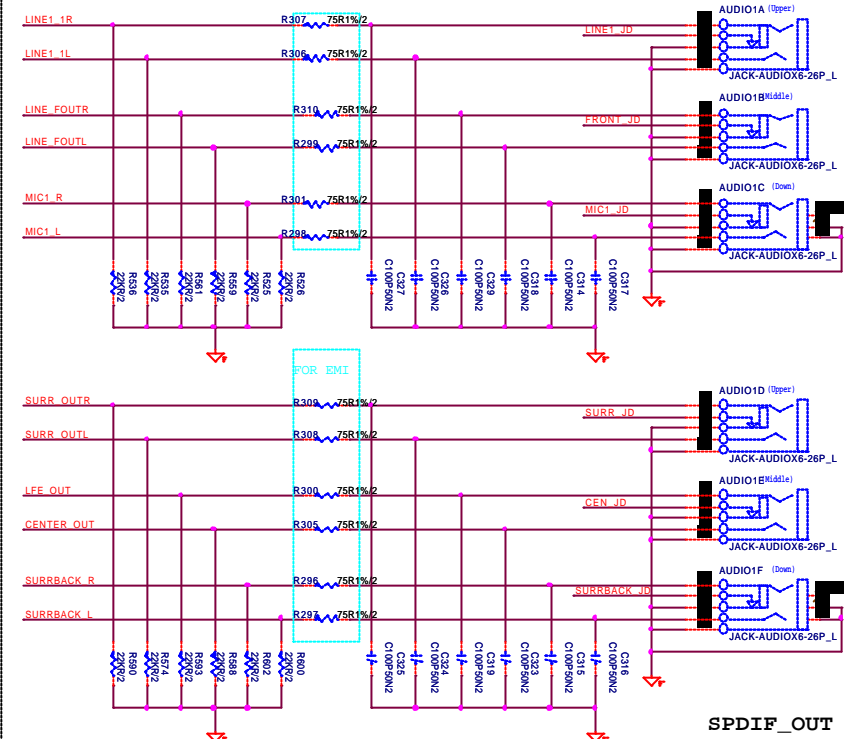
LAN CONNECTOR



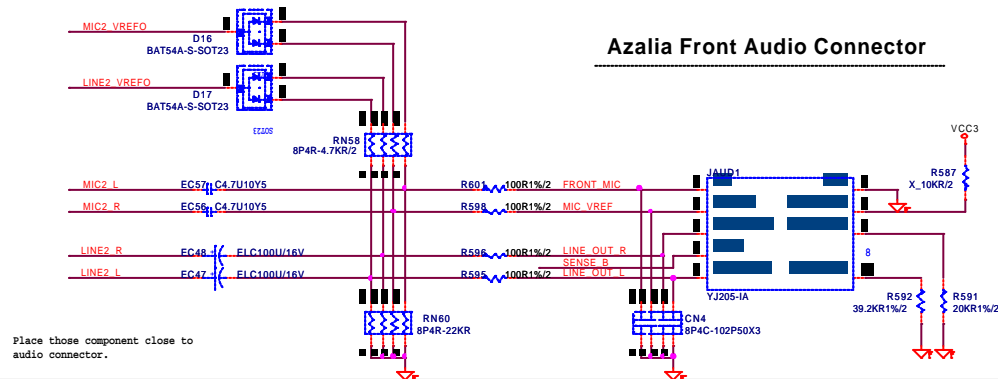
ALC883 CODEC



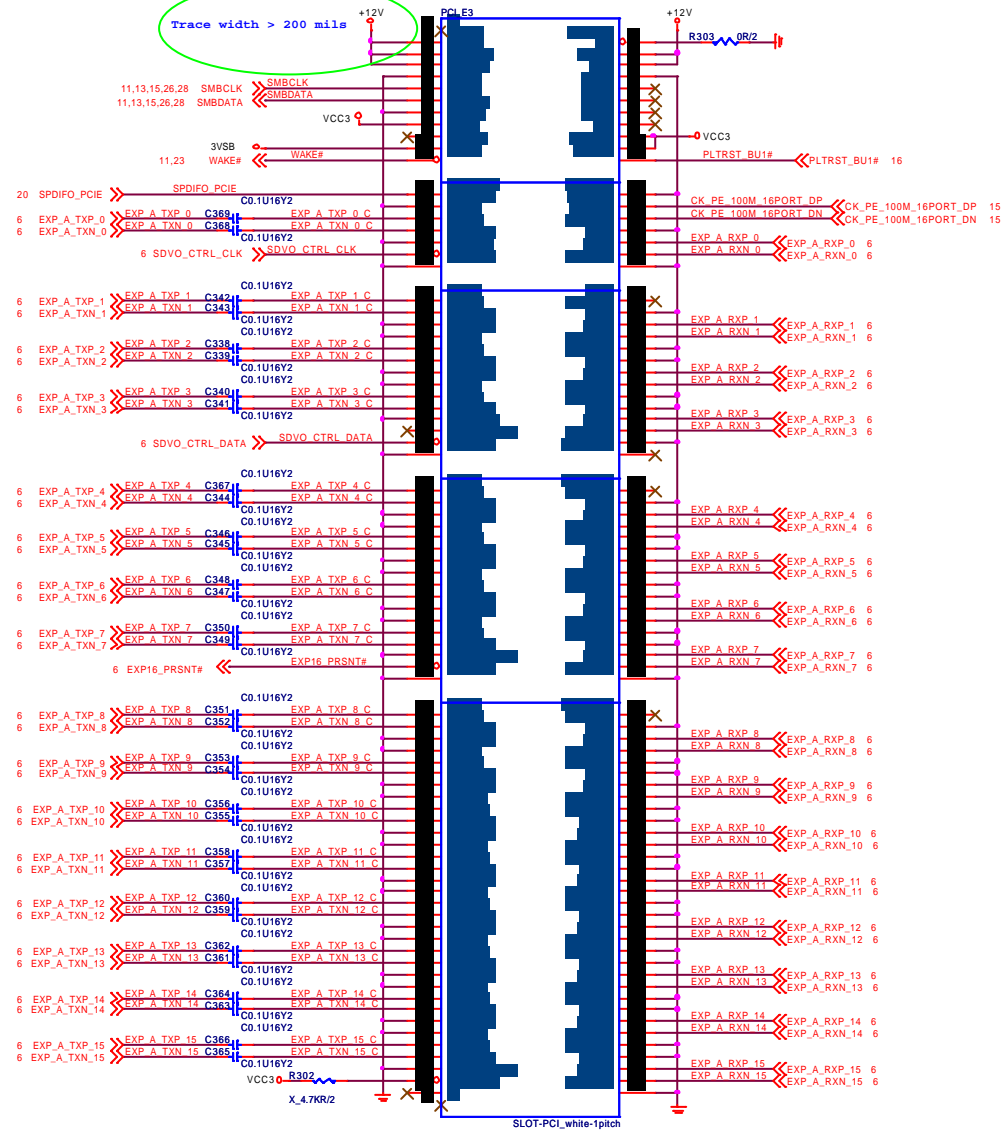
ALC883 JACK



Azalia Front Audio Connector

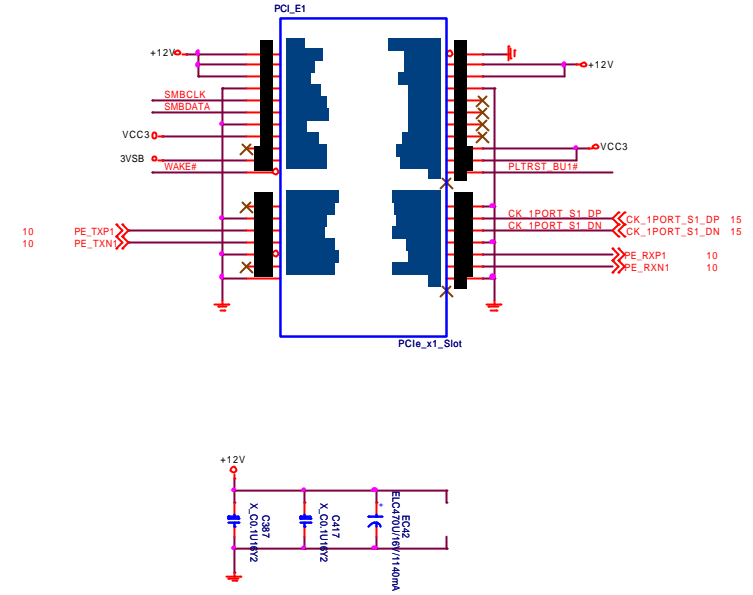


PCI_Express X16 Slot



PCI_Express X4 Slot

(Share with PCI_E x1 Slots)

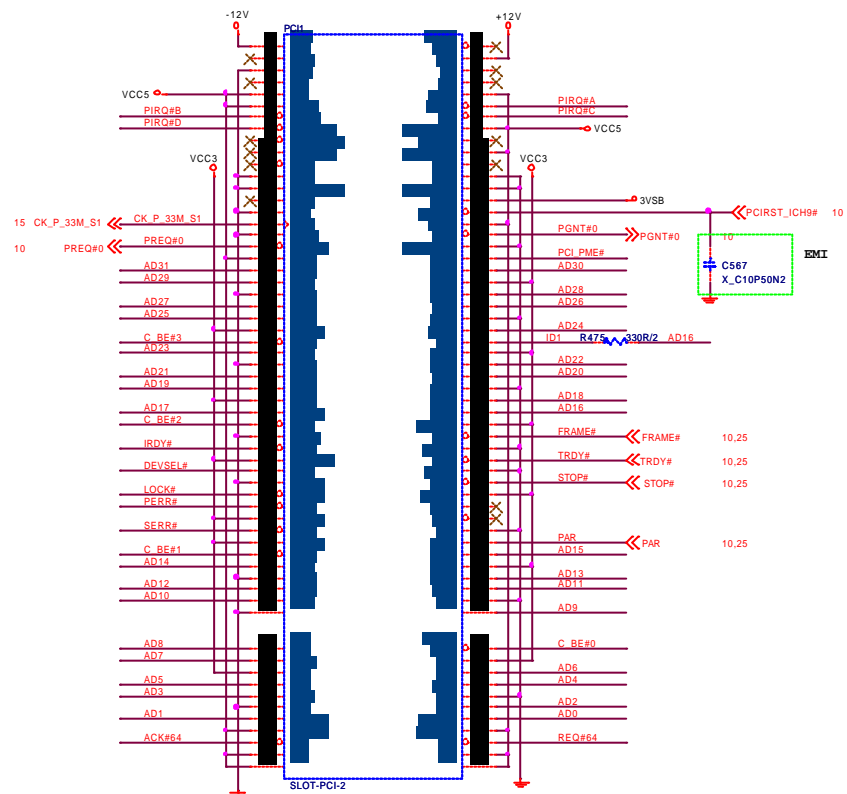


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Custom	PCIe x16, x4, x1 & Bus Switch	0A
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PCI SLOT 1 (PCI VER: 2.2 COMPLY)



```

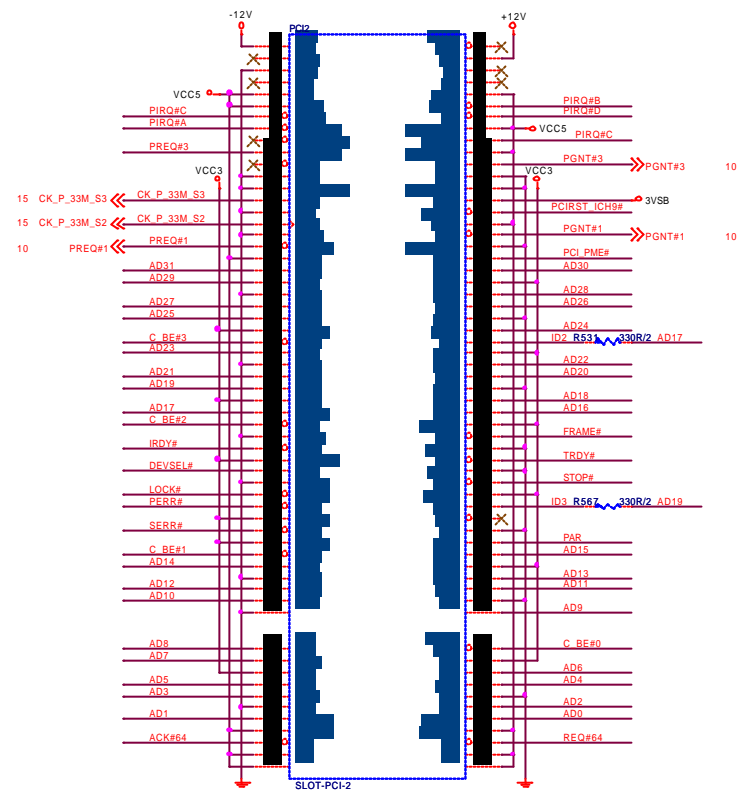
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

```

10,25 AD[31..0] << AD[31..0]

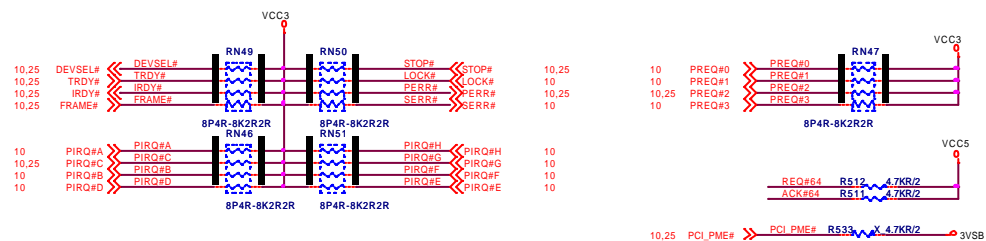
10,25 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

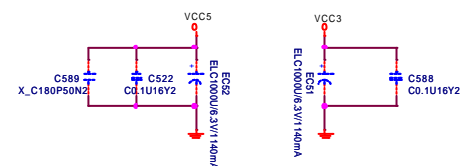


```
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B
```

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR INT'L CO.,LTD

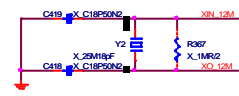
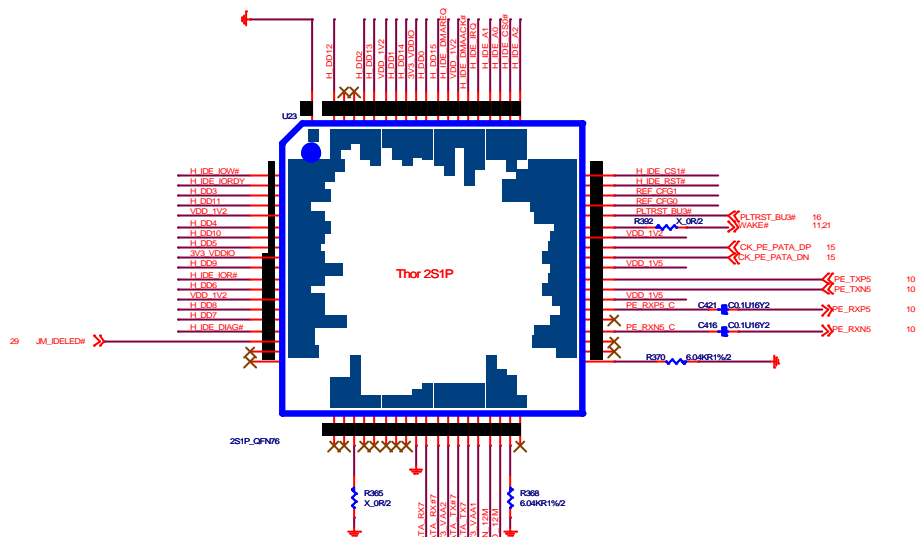
MS-7358

Size	Document Description
Custom	PCI Slot 1 & 2

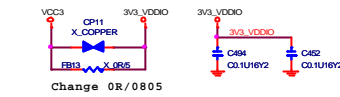
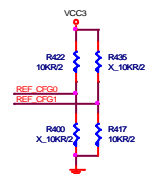
Rev	0A
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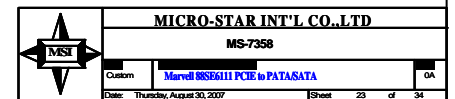
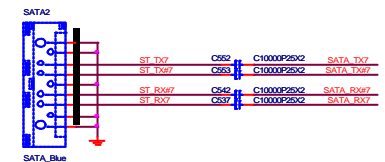
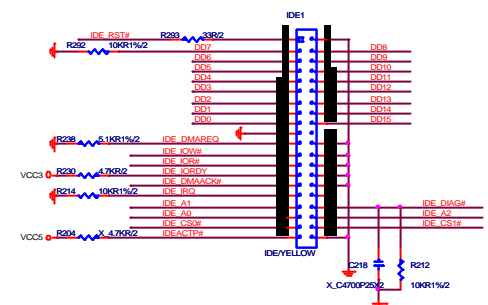
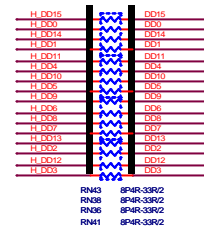
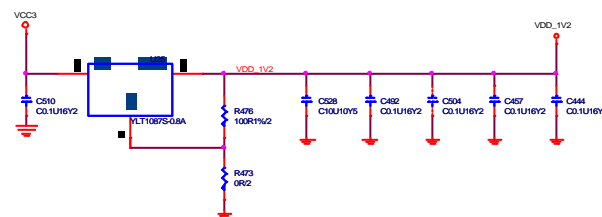
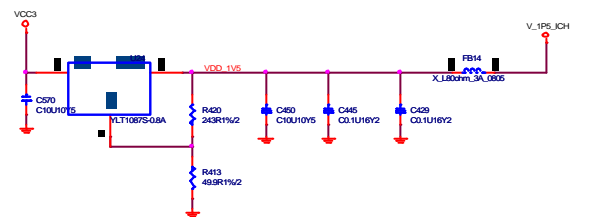
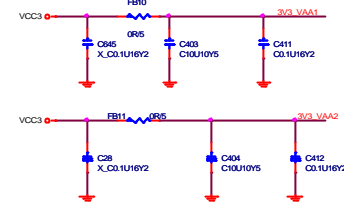
Hi-Speed PCIE to SATA/PATA Bridge



```
REF_CFG[1:0] =
00:20MHz
01:25MHz
```



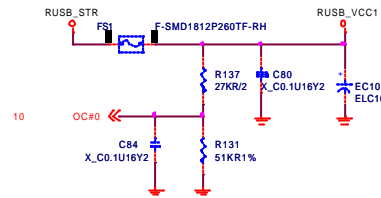
L02-8008074-J07 FOR BEAD



Rear USB Connector

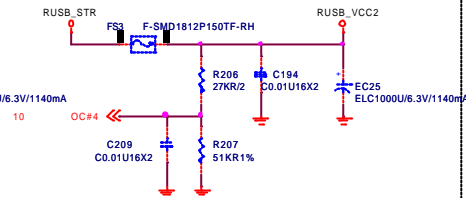
USB POWER FOR PORT 0,1

NEAR CONNECTOR

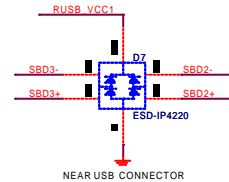
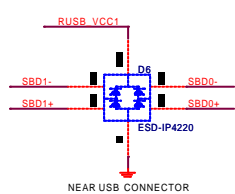
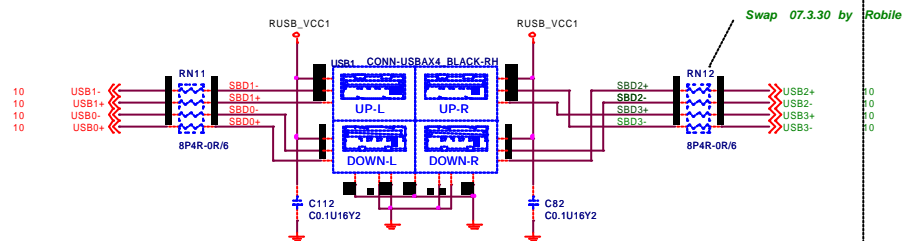


USB POWER FOR PORT 2,3,4,5

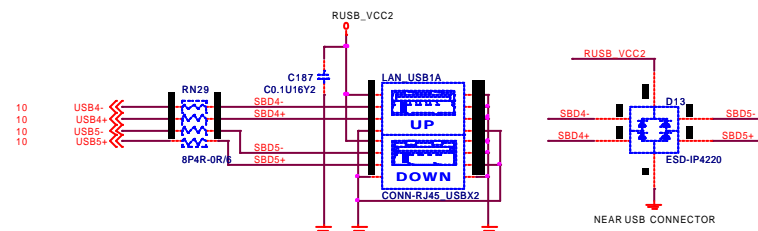
NEAR CONNECTOR



REAR USB PORT 0-3 (2x2)



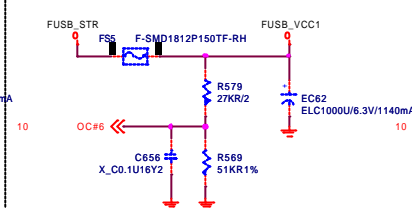
REAR USB PORT 4,5 (With LAN)



Front USB Connector

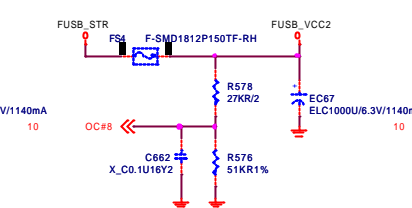
USB POWER FOR PORT 6,7

NEAR CONNECTOR



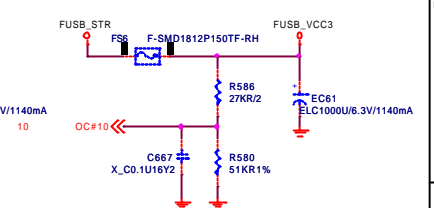
USB POWER FOR PORT 6,7

NEAR CONNECTOR

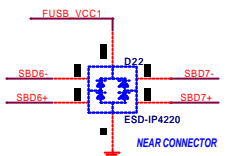
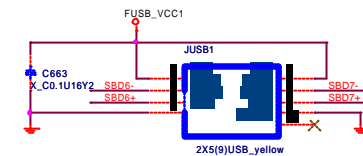


USB POWER FOR PORT 6,7

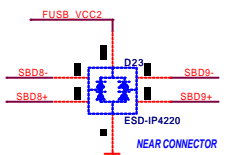
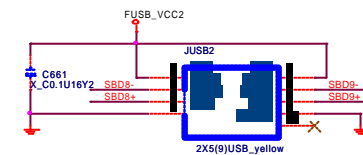
NEAR CONNECTOR



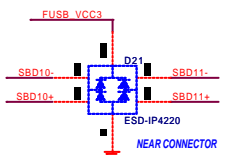
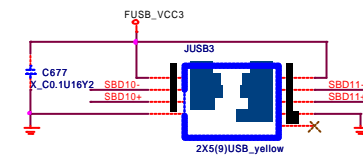
FRONT USB PORT 6,7



FRONT USB PORT 8,9



FRONT USB PORT 10,11

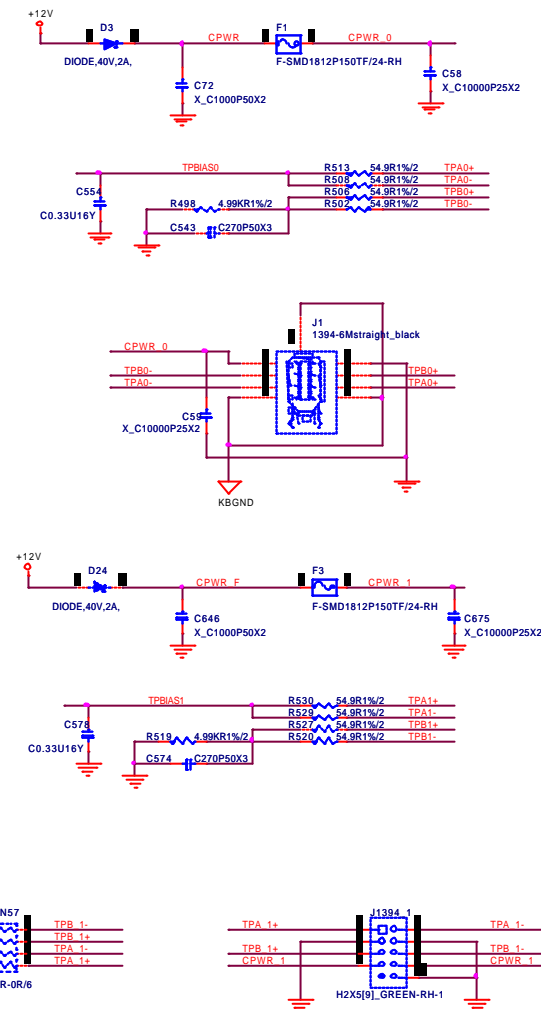
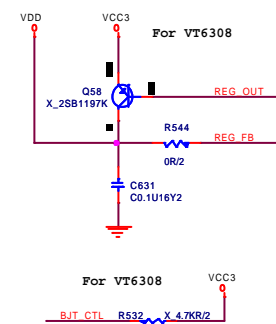
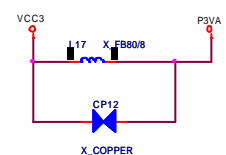
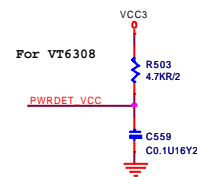
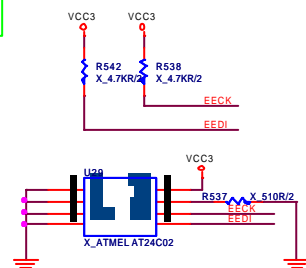
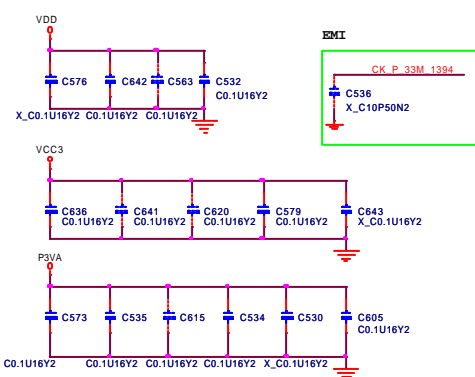
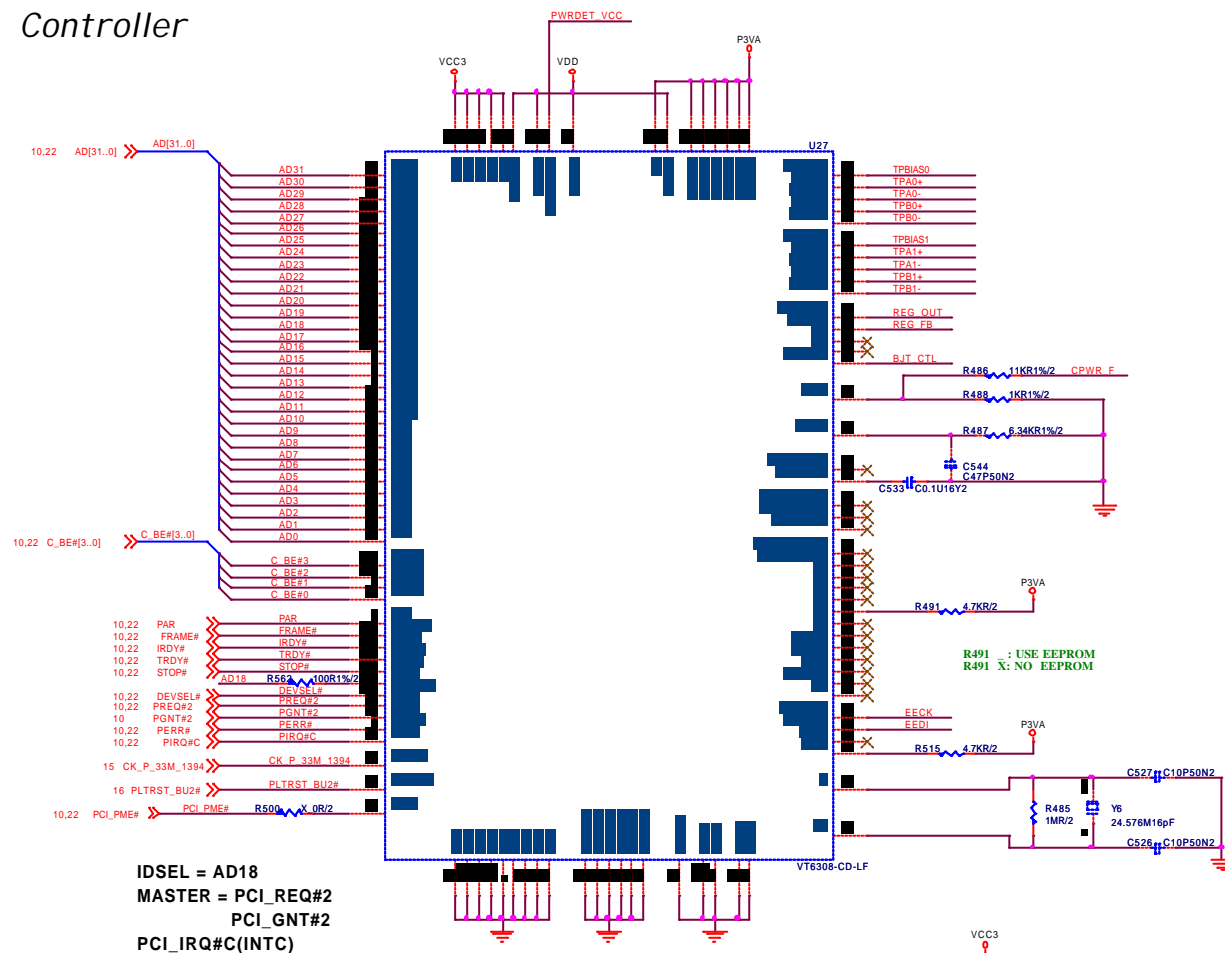


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1394a OHCI Link Layer
Controller

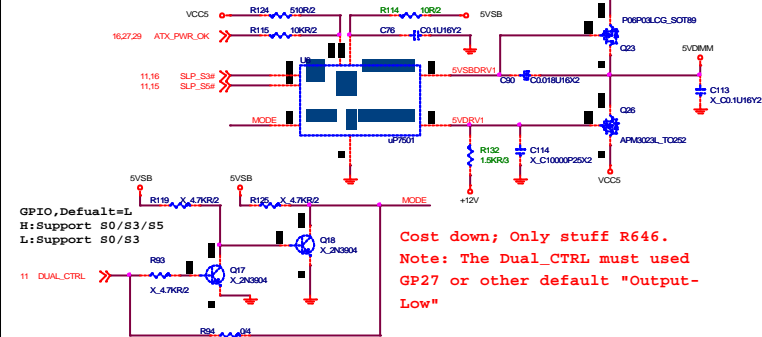


For Intel 1394 pinheader

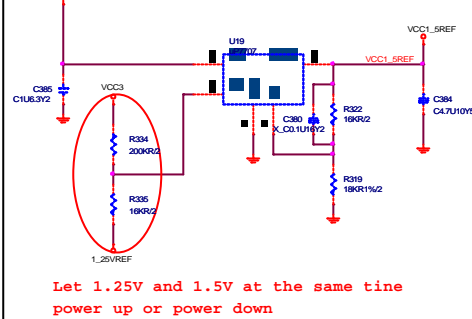


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MS-7358			
Size Custom	Document Description IEEE-1394 VIA-VT6308		Rev 0A
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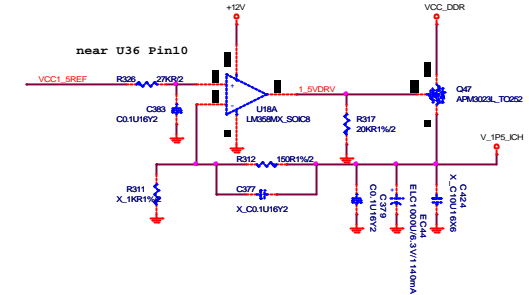
5VDIMM FOR DDR



VCC1_5REF

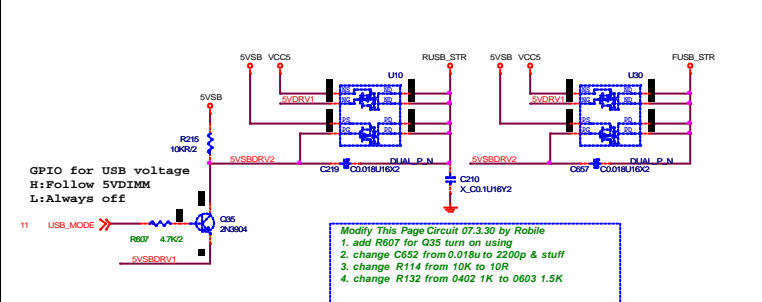


SB 1.5V 2.75A



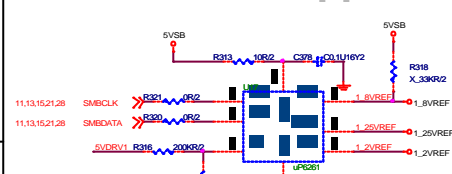
5VSB FOR Rear USB

5VSB FOR Front USB

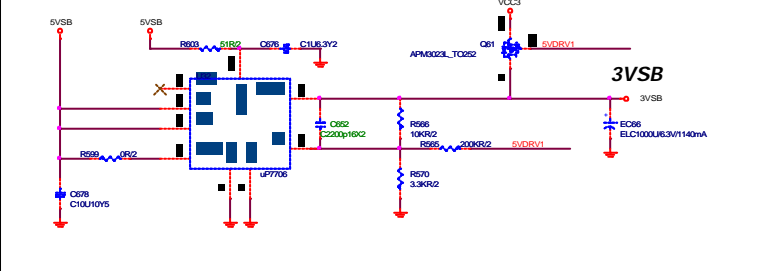
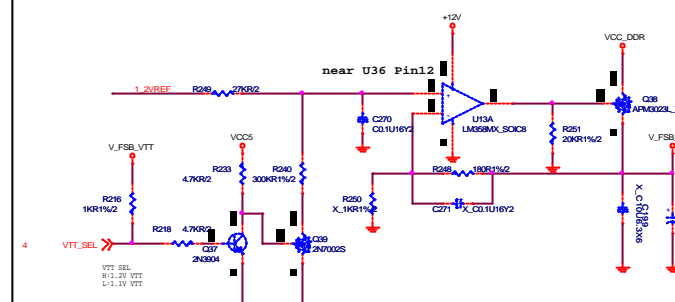


*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS
*5VSB > 4.2V POR
*Pin8 > 1.4V Enable
*Pin8 < 0.4V Disable

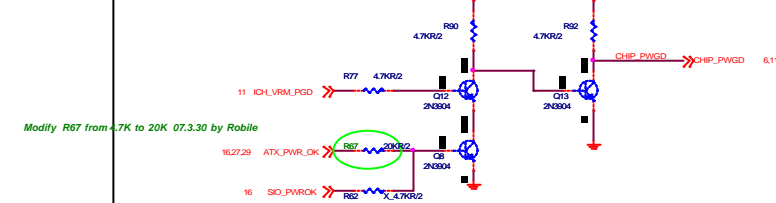
reference Voltage



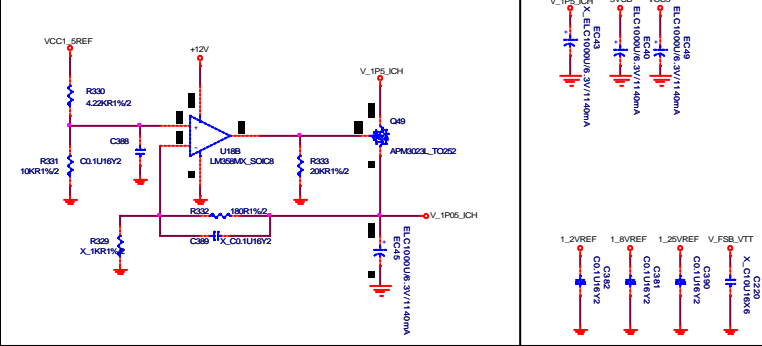
1.2V 5.8A



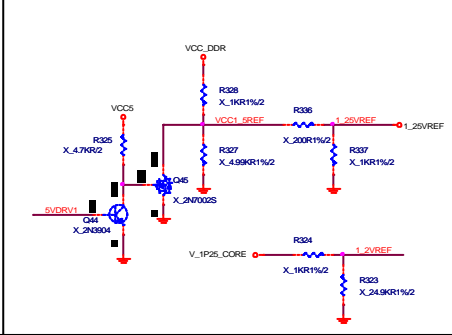
PWROK DELAY 100ms



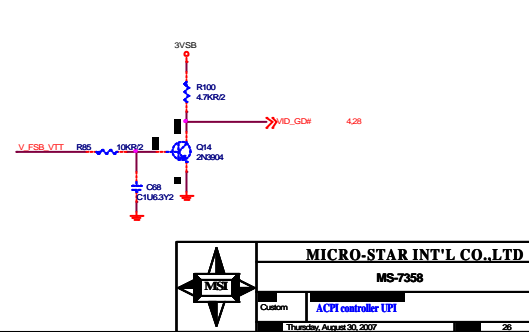
SB 1.05V 2A



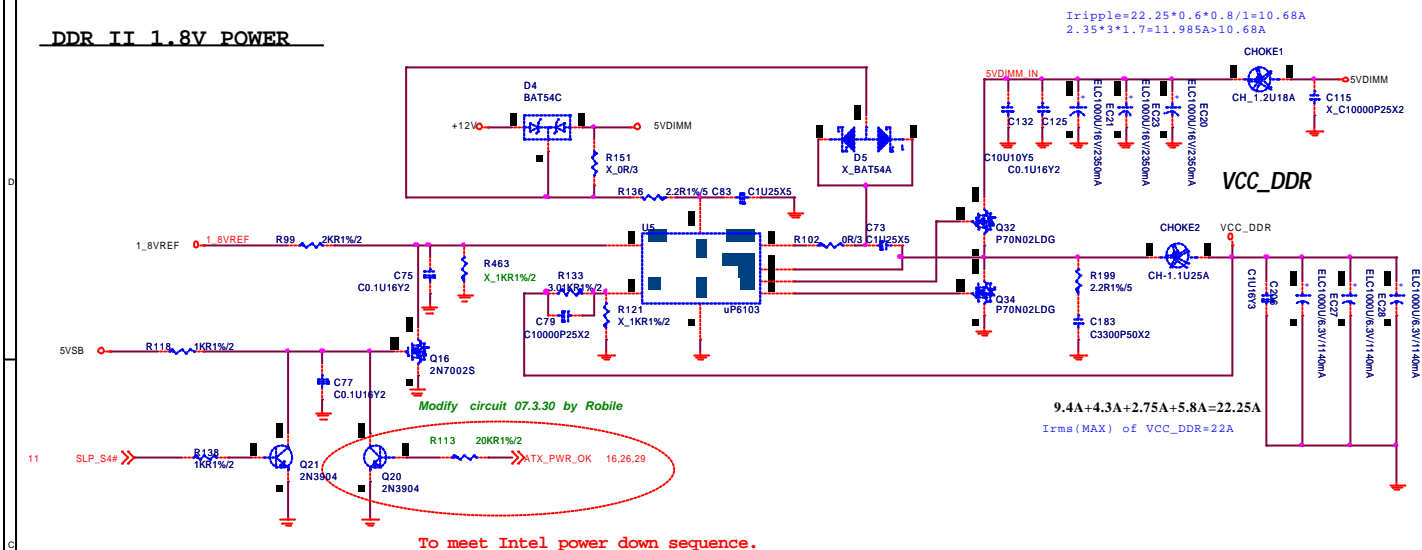
*Reserve for remove uP6261 and uP7707
*1_8REF use uP6103's internal 0.8VREF



VID before PWROK >3ms

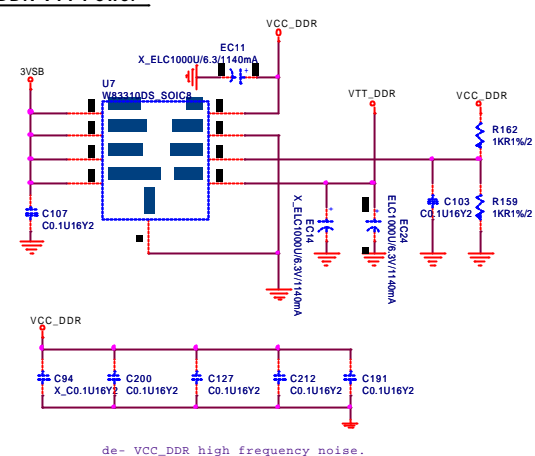


DDR II 1.8V POWER

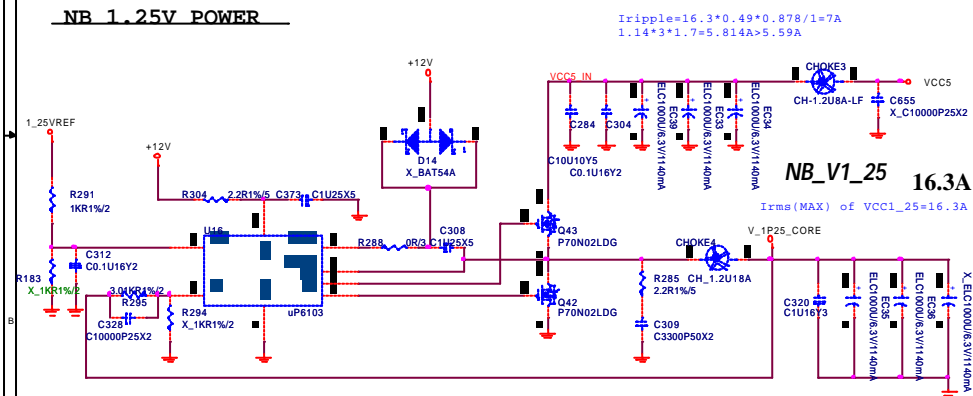


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



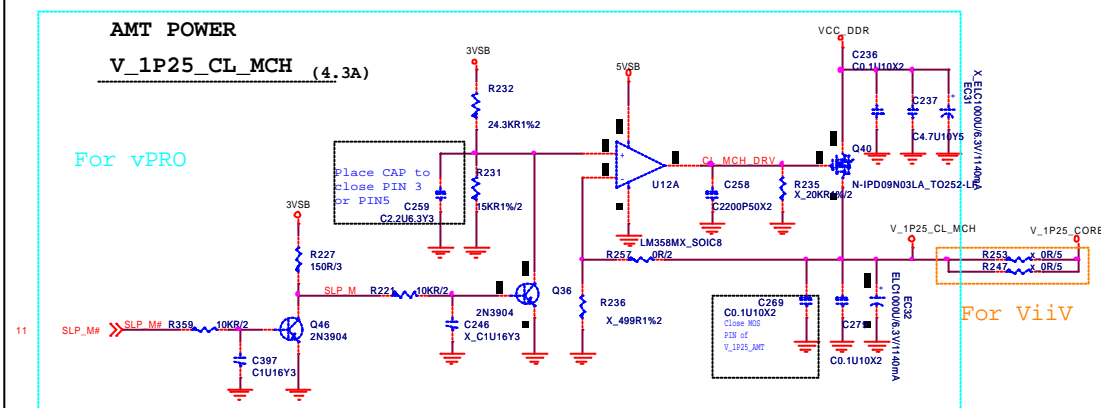
NB 1.25V POWER



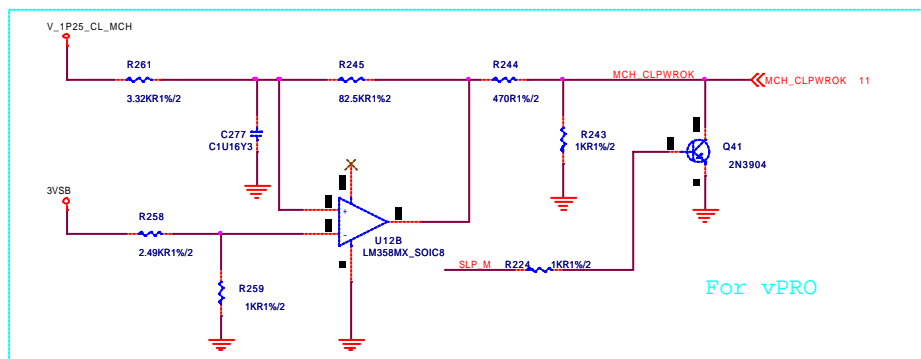
AMT POWER

V_1P25_CL_MCH (4.3A)

For vPRO



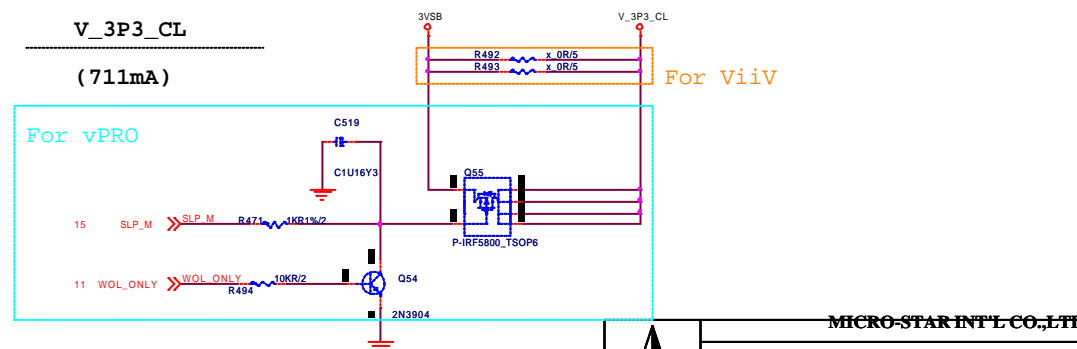
CLINK PWROK GENERATION



V 3P3 CL

(711mA)

For vPRO



~~MICRO-STAR INT'L CO., LTD~~

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Size	Document Description
Custom	NB Core Power & DDR Power

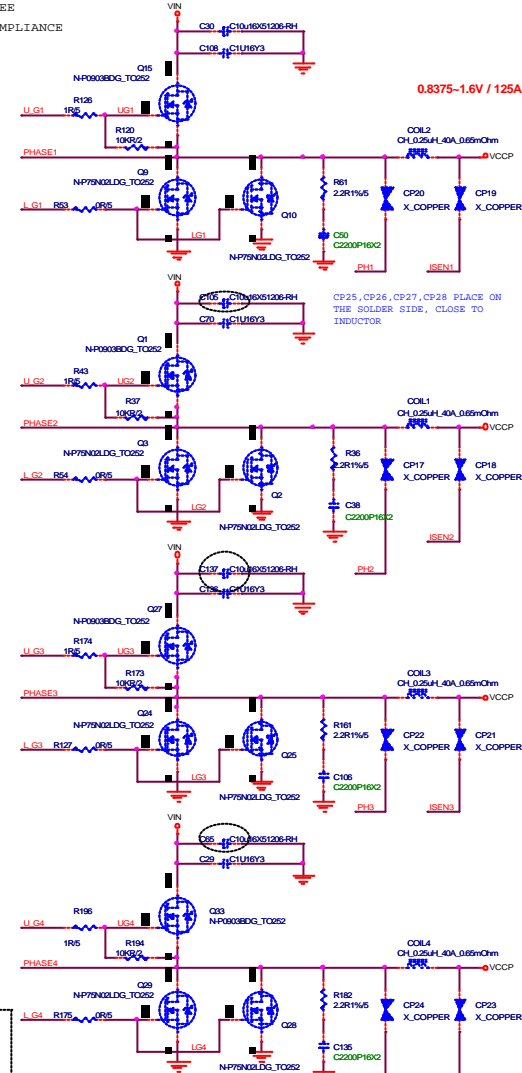
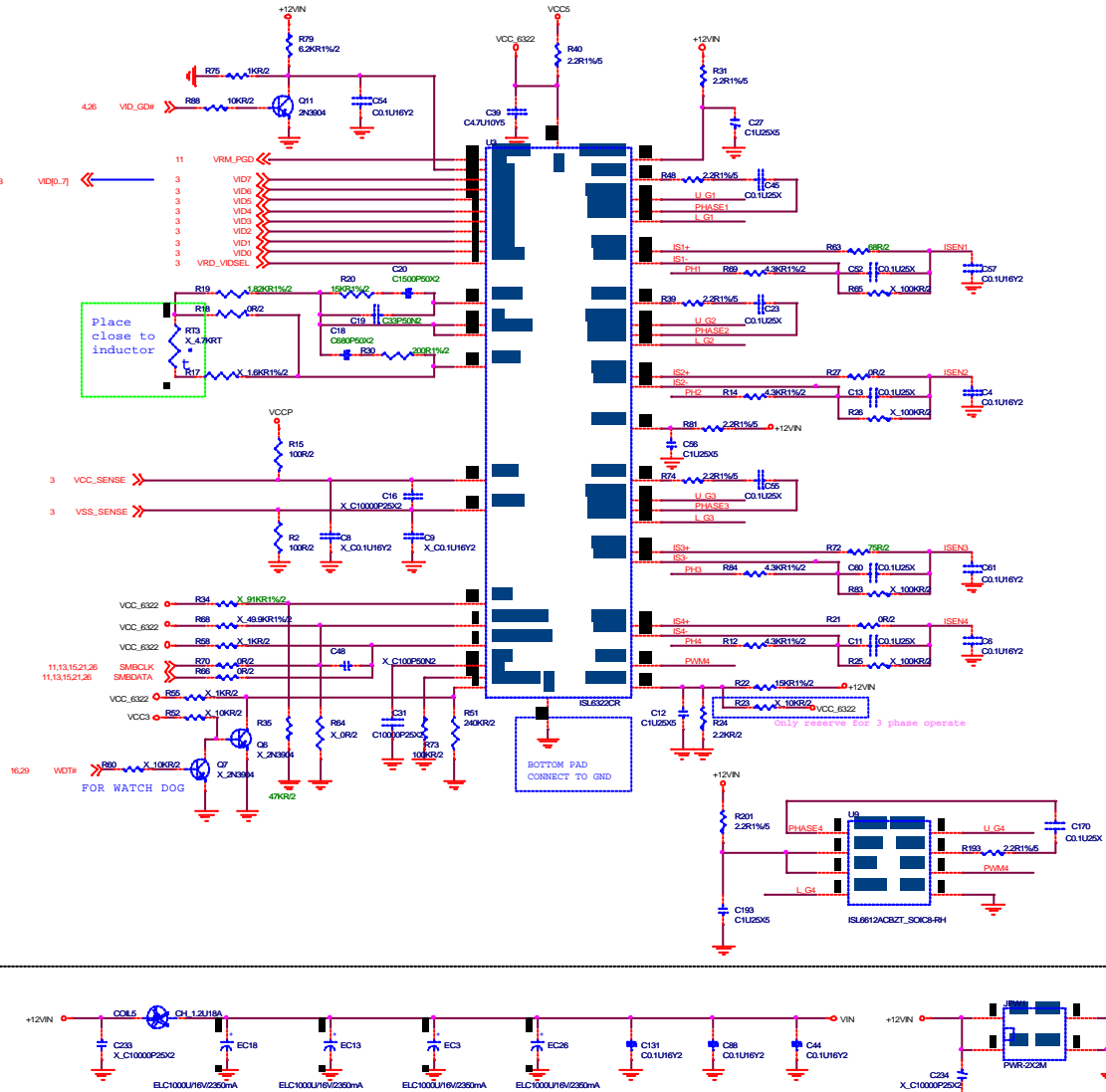
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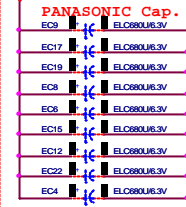
Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
CD100U2SP
CD560U40S-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD100U16EL20-2

mosfet/n-channel, P0903BDG, SMT/TO252, Rds(on)=9.5mΩ(10V/25A), Vgs(on)=1-3V, Id=50A, Ciss=1800pf, Qg=50nC, Vds=25V, Vgs=±20V, RoHS compliance.
mosfet/n-channel, P75N02LDG, SMT/TO252, Rds(on)=7mΩ(@10V, 30A), Vgs(on)=1-3V, Id=75A, Ciss=5000pf, Qg=140nC, Vds=25V, Vgs=±20V, RoHS compliance.
ESR<12mΩ, Ripplecur<2350mA, 105C, longlife change from 2000hrs to 3000hrs, KZJ
IND CHOKE, 0.25uH, 20%, DIP/8.5mm, 40A, 0.6mΩ, PEW, FERRITE, SQUARE, RoHS COMPLIANCE
IND CHOKE, 1.1uH, 20%, DIP/9mm, 25A, 1.4mΩ, 5.5T, 0.9mmx3, PEW, IRON, LEAD FREE
CAP, EL, 1000uF, 16V, Dip-8x20/3.5mm, 20%, 12mΩ, 2350mA, 105C, 3000hrs, RoHS COMPLIANCE

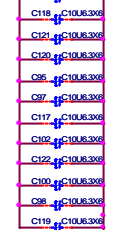


VCCP 680uF EL Capacitors

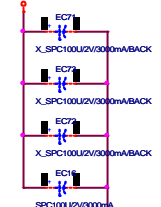


MLCC Inside Socket

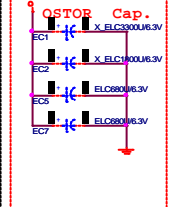
Samsung Cap.



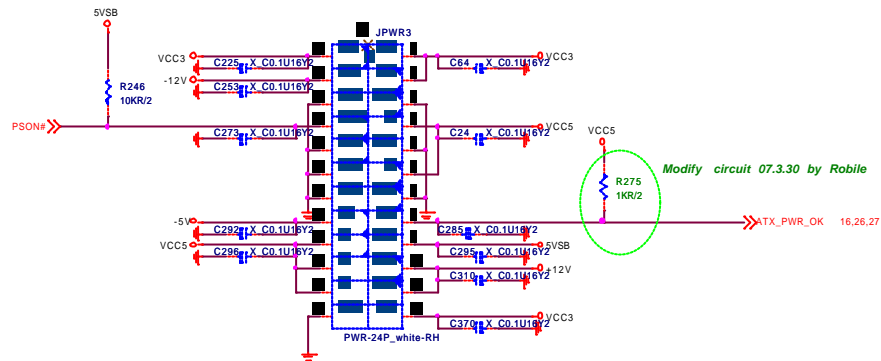
SP Capacitors



EL Capacitors



ATX POWER CONNECTOR



CHANNEL A V_SM_VTT DECOUPLING CAPS

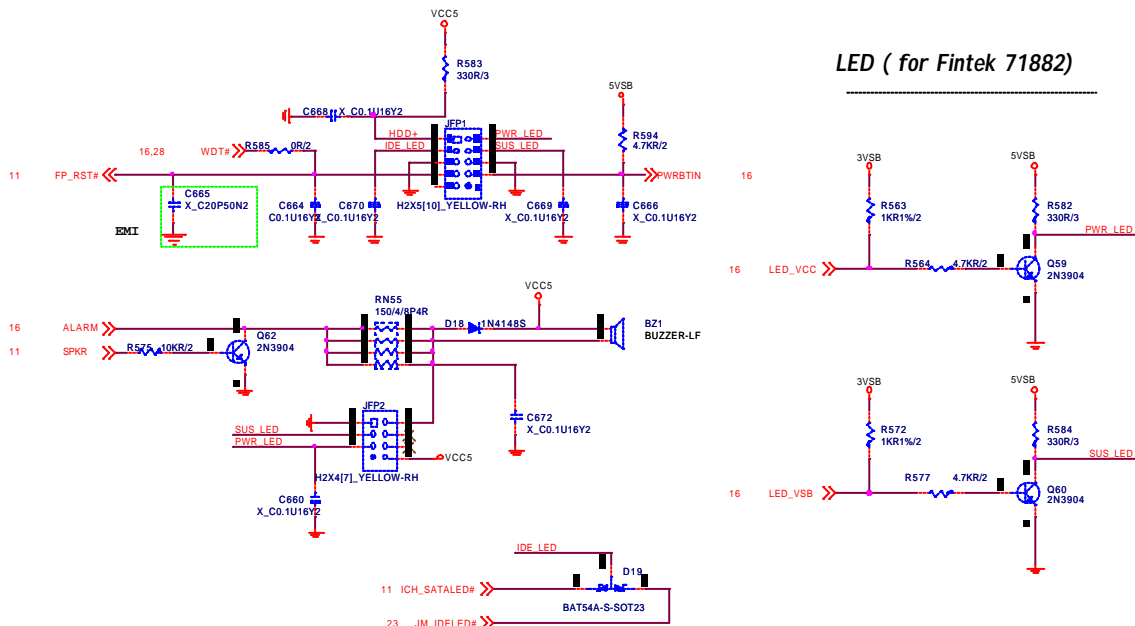
CHANNEL B V_SM_VTT DECOUPLING CAPS

FOR EMI

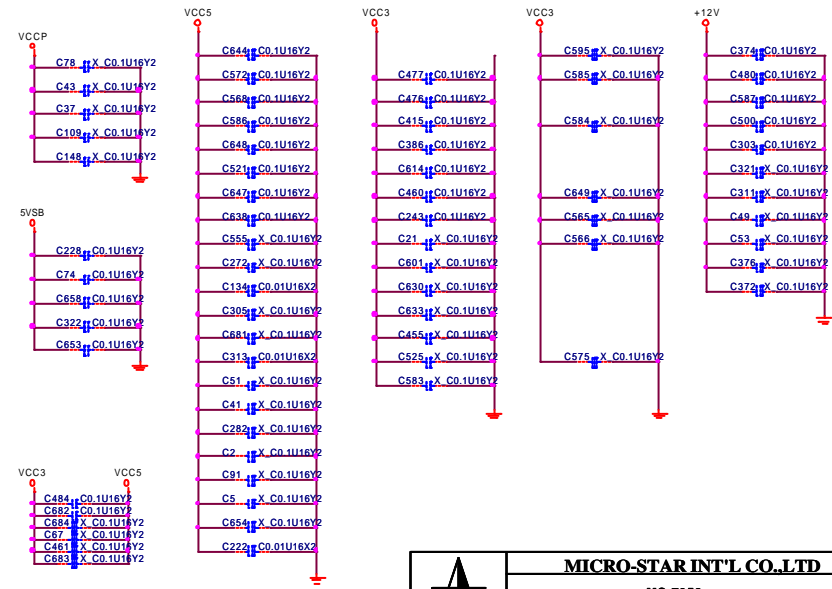


FRONT PANNEL

LED (for Fintek 71882)



Cap. for EMI & Power



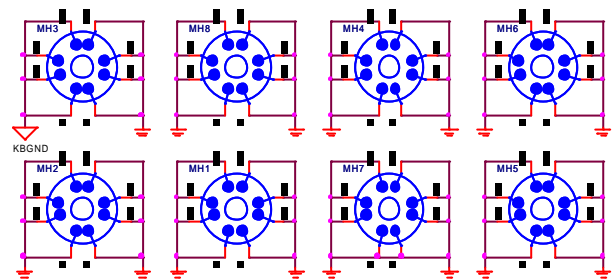
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes



Simulation

